Centre for Development of Advanced Computing (C-DAC)
A Scientific Society of Ministry of Electronics & Information Technology (MeitY), Government of India
Old Madras Road, Byappanahalli, Bengaluru
+91 8025093400
www.cdac.in

Expression of Interest (EoI)

for

Enabling Packaging, Multi-Project Wafer (MPW) Prototyping & Post Silicon Validation Services for ChipIN Centre

EoI No: C-DACB/EOI- PKG-MPW-PSV/2024-25

18 October 2024

Version 1

Contents

1 Notice Inviting Expression of Interest (EoI)

C-DAC Bangalore, a premier R&D organization and a Scientific Society under the Ministry of Electronics and Information Technology (MeitY), Govt. of India, invites Expression of Interest (EoI) from qualified and experienced vendors for offering services such as Packaging, Multi-Project Wafer (MPW) Prototyping & Post Silicon Validation for DLI onboarded companies.

As part of the Government of India's mission to strengthen the domestic semiconductor ecosystem, C-DAC Bangalore serves as a key facilitator, enabling DLI onboarded companies with empanelled vendors who offer services such as, Packaging, Multi-Project Wafer (MPW) Prototyping and Post Silicon Validation. These services are essential for companies involved in semiconductor design and development, ensuring that their innovations can be transformed into functional silicon ICs and products.

Firms may please submit their EoI in the format mentioned in the Annexure I On-Line only through Central Public Procurement Portal expressing their interest for offering Packaging/ Multi-Project Wafer (MPW) Prototyping/ Post Silicon Validation services for DLI onboarded companies.

The details are as below:

Issue of EoI	18-10-2024
EoI End Date	04-11-2024 C-DAC may cancel / amend / reissue the Expression of Interest as and when needed.

Important Notes:

- The information to be furnished by the applicants is given in Annexure-I. Interested parties can submit the EoI in the application form in Annexure-I duly filled in with all relevant supporting documents as mentioned in section 12 of EoI document.
- The EoI can be submitted On-Line only through Central Public Procurement Portal with in the deadline.
- C-DAC shall not be responsible for non-receipt / non-delivery of the EoI documents due to any reason whatsoever.
- Any queries relating to the process of on-line bid submission or queries relating to Central Public Procurement (CPP) Portal in general may be directed to the 24*7 CPP Portal Helpdesk. The contact number for the helpdesk is 1800 233 7315.
- At any time of EoI, C-DAC may carry out amendment(s) to this EoI document and/or the schedule. The amendment will be made available on the website (www.cdac.in) and will be binding on them.
- To assist in the examination, and evaluation of EoI, C-DAC, at its discretion can ask the applicant for the clarification of their EoI. The request for clarification and the response shall be in writing through email.
- C-DAC, reserves the right to visit the facilities of the applicant if required. The official(s) of C-

DAC may visit applicants facilities for the assessment.

- Applicants, if they choose, may visit C-DAC with prior appointment with the contact person as stated below prior to submission of their Expression of Interest.
- C-DAC reserves the right to accept or reject any application without assigning any reason thereof. C-DAC also reserves the right to disqualify the Applicant(s) and terminate the Agreement, if any entered into, should it be deemed so necessary at any stage on the grounds of national security.
- EoI that are incomplete in any respect or those that are not consistent with the requirements as specified in this document or those that do not adhere to formats, wherever specified may be considered non-responsive and may be liable for rejection and no further correspondences will be entertained with such applicants.
- Canvassing in any form would disqualify the applicant.
- The EoI document may be downloaded from the website, www.cdac.in and https://eprocure.gov.in/eprocure/app

For any technical clarification, please approach the following person(s):

Dr. Abey Jacob

Centre for Development of Advanced Computing (C-DAC)

No.1, Old Madras Road, Byappanahalli, Bengaluru – 560038

Contact:+91-80-25093476

Email: abeyj@cdac.in

For other clarification, please approach the following person(s):

Shri. Jyotsna Murlidhar

Centre for Development of Advanced Computing (C-DAC)

No.1, Old Madras Road, Byappanahalli, Bengaluru – 560038

Contact: +91-80-25093415

Email: mmg-blrkp@cdac.in

Competent Authority

C-DAC Bangalore

2 DISCLAIMER

1. Centre for Development of Advanced Computing, Bangalore (herein after called C-DAC) has prepared this Expression of Interest Document ("EoI Document") solely to invite vendors who possess the expertise and capabilities to provide the services mentioned in section 1 through empanelled vendors. While C-DAC has taken due care in the preparation of information contained herein and believes it to be accurate, neither C-DAC or any of its Authorities or Agencies, nor any of their respective officers, employees, agents or advisors give any warranty ormake any representations, express or implied as to the completeness or accuracyof the information contained in this document or any information which may be provided in association with it.
2. This information is not intended to be exhaustive and interested parties are required to make their own inquiries in order to submit the EoI. The information isprovided on the basis that it is non–binding on C-DAC, any of its authorities or agencies or any of their respective officers, employees, agents or advisors.
3. C-DAC reserves the right not to proceed with the EoI process at any stage without assigning any reasons thereof, or to alter the timelines reflected in this document or to change the process or procedure to be applied. It also reserves the right to decline to discuss the EoI further with any party submitting an EoI.
4. C-DAC will not be liable to pay / reimburse any cost / losses / expenses / penalties / damages of whatsoever nature to any person (s) / entity (ties) submitting the EoI.
5. This EoI Document is neither an agreement nor an offer and is only an invitation by C-DAC to the entities that are qualified to submit their Expression of Interest asstated in the Notice Inviting EoI.
6. The purpose of this Notice Inviting EoI Document is to invite interested applicants EoI who possess the expertise and capabilities to offer Packaging/ Multi Project Wafer (MPW) Prototyping/ Post Silicon Validation Services to DLI on-boarded companies.
7. The issue of this EoI does not imply that C-DAC is bound to select any partner.
8. This EoI will be open till further notice and any company who wishes to deliver Packaging/ Multi Project Wafer (MPW) Prototyping/ Post Silicon Validation services can apply for obtaining the/ same.

3 INTRODUCTION

Centre for Development of Advanced Computing (C-DAC) is the premier R&D organization under the Ministry of Electronics and Information Technology (MeitY), Govt. of India, for carrying out R&D in IT, Electronics and associated areas. C-DAC has today emerged as a prominent R&D organization in IT&E (Information Technologies and Electronics) in the country working on strengthening national technological capabilities in the context of global developments in the field and responding to change in the market need in selected foundation areas.

C-DAC's expertise spans a wide range of technologies, establishing it as a leader in India's digital transformation. The organization excels in areas such as High-Performance Computing (HPC), Internet of Things (IoT), VLSI, Artificial Intelligence (AI), Cyber Security, Blockchain, and e-governance. Notably, C-DAC has played a pivotal role in India's supercomputing initiatives, including the PARAM series, which has positioned the country as a global player in HPC. Additionally, C-DAC is at the forefront of embedded systems and system-on-chip (SoC) design, driving innovation in automation, robotics, and Industrial IoT applications. C-DAC has also developed cutting-edge solutions in healthcare, including telemedicine platforms, bioinformatics tools, and medical imaging technologies, which are transforming healthcare delivery, especially in remote and rural areas. The organization's focus on 5G and wireless communications has led to the creation of indigenous technologies that are strengthening India's telecommunications infrastructure. Its contributions to power electronics, energy measurement systems, and smart grid technologies support the nation's growing emphasis on energy efficiency and sustainable solutions. Moreover, C-DAC is involved in Quantum Computing research, enabling the development of next-generation computational capabilities, and plays a key role in e-governance projects, critical to the digital transformation of government services. By consistently advancing in these diverse technological areas, C-DAC remains a cornerstone of India's IT and Electronics landscape.

With a fervent vision to make India a high-end Very Large Scale Integration (VLSI) design destination, Ministry of Electronics & Information Technology (MeitY) has initiated Special Manpower Development Programme for Chips to System programme. This programme brings in a culture of System on Chip / System designing by developing working prototypes with societal applications. It enables the academic institutions to develop specialized manpower in the area of VLSI/ microelectronics and Chip to System development and broadens the base of ASIC / IC designing in the country.

3.1 NATIONAL EDA TOOL GRID - ChipIN

The Ministry of Electronics and Information Technology (MeitY), Government of India, has established the National EDA Tool Grid, known as the ChipIN Centre, at C-DAC Bangalore. This facility is dedicated to supporting the semiconductor design community across the country. It serves as a one-stop solution, providing fabless chip designers from startups, MSMEs, and academia with access to semiconductor design tools, fabrication services, and virtual prototyping hardware labs.

ChipIN Centre is a cloud-supported, centralized facility that hosts state-of-the-art EDA tools covering the entire chip design cycle. It also offers aggregated services for fabricating designs at various foundries. The Centre plays a critical role in advancing India's chip design ecosystem by providing

Multi-Project Wafer (MPW) support to academic institutions, startups, and MSMEs, enabling them to access both Indian and international foundries.

In addition, the Centre offers centralized EDA design tools from leading vendors such as Synopsys, Cadence, Siemens, KeySight, and Silvaco under the Design Infrastructure Support (DIS) for the DLI scheme. It also provides essential design services, including fabrication compliance checks, validation, design integration, coordination with packaging firms, and support for chip characterization and prototyping.

The facility aims to promote innovation by creating a reusable IP core repository and offering training on EDA tools. It also features a Virtual Prototyping Lab (SMARTLAB) at NIELIT Calicut, specifically designed for imparting VLSI design training.

3.2 DESIGN LINKED INCENTIVE (DLI) SCHEME

Semiconductors are at the heart of all electronic products and constitute a significant share in the Bill of Material (BOM). The National Policy on Electronics 2019 aims to position India as a global hub for Electronics System Design and Manufacturing (ESDM) and envisions creation of a vibrant semiconductor chip design ecosystem in the country. With an exceptional talent pool of 20% of world's semiconductor design engineers and thousands of chips designed by them every year in the country, India is poised for growth to achieve self-reliance and technology leadership in semiconductor design sector. Ministry of Electronics and Information technology has announced the Design Linked Incentive (DLI) Scheme to offset the disabilities in the domestic industry involved in semiconductor design in order to not only move up in value-chain but also strengthen the semiconductor chip design ecosystem in the country. C-DAC is responsible for implementation of the DLI Scheme as Nodal Agency. The Design Linked Incentive (DLI) Scheme aims to offer financial incentives as well as design infrastructure support across various stages of development and deployment of semiconductor design(s) for Integrated Circuits (ICs), Chipsets, System on Chips (SoCs), Systems & IP Cores and semiconductor linked design(s) over a period of 5 years.

3.3 OBJECTIVES OF DLI SCHEME.

- Nurturing and facilitating the growth of the domestic companies, Startups and MSMEs.
- Achieving significant indigenization in semiconductor content and IPs involved in the electronic products deployed in the country, thereby facilitating import substitution and value addition in electronics sector.
- Strengthening and facilitating access to semiconductor design infrastructure for Startups and MSMEs.

The objective of this EoI is to identify and engage with vendors who possess the expertise and capabilities to enable the Packaging, Multi-Project Wafer (MPW) Prototyping & Post Silicon Validation services. By doing so, C-DAC Bangalore aims to bring the semiconductor designs of organizations under ChipIN programme to market efficiently and effectively.

C-DAC invites Expressions of Interest (EoI) from companies/firms (Applicants) through the Central Public Procurement Portal. The applicants should have experience in Packaging, Multi-Project Wafer

(MPW) Prototyping, or Post-Silicon Validation and must meet the eligibility criteria set out in Section 10.1

3.4 SCOPE OF SERVICES

The scope of services that can be offered under the EoI includes the following key areas:

3.4.1 PACKAGING:

Service Category	Description	Scope of Services
Comprehensive Packaging	Providing end-to-end packaging solutions that adhere to industry standards for various semiconductor devices.	- Custom package design, Quad Flat No Lead (QFN), Ball Grid Array (BGA), Thin Small Outline Package (TSOP), Dual In-line Package (DIP), Quad Flat package (QFP), Small Outline Package (SOP), Plastic Leaded Chip Carrier (PLCC), Material selection, Packaging process development, etc.
Advanced Packaging	Offering advanced technologies to enhance the performance, reliability, and efficiency of fabricated chips.	- 2.5D and 3D IC packaging, Wafer Level Packaging (WLP), etc.
Die Attach and Bonding Services	Attaching the semiconductor die to the substrate or lead frame and creating electrical connections through wire bonding or flip-chip bonding	-Die attach material selection (e.g: solder, adhesive), Flip-chip, Wire bonding, etc.
Thermal Management	Implementing thermal solutions to ensure optimal heat dissipation and maintain device reliability.	- Thermal interface materials, Heat spreaders, Cooling solutions, etc.
Assembly Services	Providing assembly services for various package types, including surface-mount and through-hole components.	- Component placement, Soldering, Inspection and quality control, etc.
Environmental Testing	Conducting environmental stress tests to ensure packaging resilience under different conditions.	- Temperature cycling, Humidity testing, Mechanical shock and vibration testing, etc.
Package Rework and Repair	Services to rework or repair faulty or damaged packages without the need for full re-fabrication.	-Lead/terminal repair, Re-encapsulation, etc.

3.4.2 MULTI-PROJECT WAFER (MPW) PROTOTYPING:

Service	Description	Scope of Services
Prototype Fabrication	Facilitating access to MPW services that allow companies to fabricate prototypes at reduced costs.	- Multi-Project Wafer (MPW) runs, Small volume prototyping, Mask generation, etc.
Design Validation	Enabling faster design iterations and validation before full production.	- Pre-silicon validation, DRC and LVS checks, Design rule compliance, etc.
Process Customization	Offering process customization to meet specific design requirements during MPW prototyping.	- Customized process nodes, Process parameter tuning, Test structure integration, etc.
IP Integration	Supporting integration of third-party IP cores into prototypes.	- IP core licensing, IP core validation, SoC integration, etc.
DFT (Design for Test)	Providing DFT services to enhance testability and reduce the cost of testing prototypes.	- Scan insertion, BIST (Built-in Self-Test) integration, JTAG implementation, etc.

3.4.3 POST-SILICON VALIDATION (BENCH LEVEL):

Service	Description	Scope of Services
Hardware design and manufacturing	Develop and manufacture device test plan specific hardware to validate performance against specifications on Bench level.	HW boards
Electrical Characterization	Conducting electrical tests to validate performance against specifications.	- I-V characterization, Timing analysis, Power consumption measurement, etc.
Functional Testing	Verifying the functional correctness of fabricated chips under various conditions.	- Logic testing, Memory testing, Functional coverage analysis, etc.
Power Integrity and Noise Testing	Ensuring the power delivery network (PDN) performance and noise levels meet design requirements.	-Power supply noise analysis, voltage droop testing, decoupling analysis, etc.
Bench-Level Validation	Testing chips within their target systems to ensure proper integration and functionality.	- Bench-level testing, Interoperability testing, Power-on validation, etc.
Thermal Characterization	Assessing thermal performance under different conditions using thermal chambers or localized heating systems.	-Thermal resistance measurement, Junction temperature monitoring, Heat dissipation analysis, etc.
Failure Analysis	Identifying and analyzing failure mechanisms at the bench using tools like SEM (Scanning Electron Microscopy) or FIB (Focused Ion Beam).	-Defect localization, Fault isolation, Root cause analysis, etc.
Reliability Assessment	Conducting reliability tests like electro migration analysis and burn-in tests at the bench level.	-Burn-in testing, Electro migration analysis, Temperature/voltage stress tests, etc.

3.4.4 POST-SILICON VALIDATION (SYSTEM LEVEL):

Service	Description	Scope of Services
Hardware design and manufacturing	Develop and manufacture device test plan specific hardware to validate performance against specifications.	HW boards
Electrical Characterization	Conducting electrical tests to validate performance against specifications.	- I-V characterization, Timing analysis, Power consumption measurement, etc.
System-Level Validation	Testing chips within their target systems to ensure proper integration and functionality.	- System-level testing, Interoperability testing, Power-on validation, etc.
Reliability Assessment	Conducting system-level stress tests to ensure long-term reliability under real-world operating conditions.	- System stress testing, long-term reliability data, failure mode analysis, etc.
Custom Test Development	Creating system-specific test setups and custom hardware to validate system-level functionality.	- Custom test setup, hardware integration, test program creation, etc.

3.4.5 POST-SILICON VALIDATION (ATE):

Service	Description	Scope of Services
Wafer level test hardware design and manufacturing	Develop and manufacture device test plan specific hardware to validate performance against specifications.	HW boards
Package level test hardware design and manufacturing	Develop and manufacture device test plan specific hardware to validate performance against specifications.	HW boards
Test program development for wafer level and package level test solutions	Develop test programs that meet production level test coverage and quality standards	ATE test programs
Functional Testing	Verifying the functional correctness of fabricated chips under various conditions.	- Logic testing, Memory testing, Functional coverage analysis, etc.
Electrical Characterization	Conducting electrical tests to validate performance against specifications.	- I-V characterization, Timing analysis, Power consumption measurement, etc.
Failure Analysis	Automated defect isolation using fault localization techniques via ATE systems.	- Defect localization, Failure mode analysis, Automated fault isolation, etc.
Test program qualification for High volume manufacturing production release	Evaluate the test solution to ensure production worthiness	- Qualification report

3.4.6 POST-SILICON PACKAGE AND PRODUCT QUALIFICATION:

Service	Description	Scope of Services
Hardware design and manufacturing to enable package and product level qualification	Develop and manufacture device test plan specific hardware to perform qualification tests.	HW boards
Test program (ATE) development to perform tests at intermediate read points during qual process.	Develop test programs that meet production level quality standards	ATE test programs
Run product through all the device category specific standard JEDEC Qualification processes	Evaluate the device's package and product against the industry standard qualification requirement.	- Qualification report
Custom Test Development	Developing tests for packaging-specific requirements (e.g., thermal cycling, shock testing).	- Custom qualification tests, Packaging-specific stress tests, Product lifecycle analysis, etc.
OSAT (Outsourced Semiconductor Assembly and Test) Support	Includes packaging, final testing, and product qualification services provided by third-party vendors.	- Packaging, Final testing, Qualification services, etc.

4 WHO CAN APPLY

- Vendors with a proven track record in semiconductor Packaging, MPW prototyping, and Post-Silicon Validation.
- Organizations that possess the necessary infrastructure, technical expertise, and experience to support advanced semiconductor projects.
- Vendors willing to collaborate with C-DAC Bangalore to provide high-quality services to the DLI and C2S ecosystem.

5 EMPANELMENT PROCESS

- Selected applicants will be empaneled with C-DAC Bangalore and will have the opportunity to work closely with the onboarded organizations under ChipIN programme. The empanelment process will involve a thorough evaluation of the vendor's capabilities, experience, and alignment with the program's objectives.
- Validity of empanelment will be till December 2026

6 SCHEDULE FOR EOI

The details for submitting the EoI are furnished below.

6.1 DETAILS FOR SUBMITTING EOI

The bidders may please note that the bids are required to be submitted 'On-Line' only through: https://eprocure.gov.in/eprocure/app The bidders are required to submit soft copies of their bids electronically (PDF files), using valid Digital Signature Certificates. The bid in hard copy form will not be accepted. The bidders are advised to note and take care of formalities for registration and on-line submission of bids through https://eprocure.gov.in/eprocure/app

For any technical clarification, please approach the following person(s):

Dr. Abey Jacob

Centre for Development of Advanced Computing (C-DAC)

No.1, Old Madras Road, Byappanahalli, Bengaluru – 560038

Contact:+91-80-25093476 har

Email: abeyj@cdac.in

For other clarification, please approach the following person(s):

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No.1, Old Madras Road, Byappanahalli, Bengaluru – 560038

Contact: +91-80-25093415

Email: mmg-blrkp@cdac.in

7 ROLES OF C-DAC

- C-DAC Bangalore identifies industry-leading vendors who specialize in packaging, MPW prototyping, and post-silicon validation. Through a empanelment process, C-DAC ensures that only the most capable and reliable vendors are selected, guaranteeing high-quality services for the onboarded companies.
- C-DAC encourages collaboration between the onboarded companies and vendors, fostering an environment of innovation and knowledge sharing. By acting as a central point of contact, C-DAC helps create synergies that drive the success of the DLI program.

8 APPLICANTS ELIGIBILITY CRITERIA

This process is open to all applicants who fulfil the Qualification criteria as set out in Section 10.1 of this document. The applicants should furnish information on the lines of Section 10.1 in their EoI proposal.

9 INSTRUCTION TO APPLICANTS

The EoI is to be submitted in the manner prescribed below. All the information as detailed below is to be submitted through Central Public Procurement Portal.

1. Documents to be furnished
    a. Applicant's Expression of Interest (Format - 1)
    b. Application Form (Format - 2)
    c. Experience of the Organization (Format - 3)
    d. Declaration (Format - 4)
2. Important Notes
    a. At any time prior to the deadline for submission of EoIs, C-DAC may modify any part of this document. Such change(s) if any may be in the form of an addendum / corrigendum and will be uploaded in C-DAC website https://www.cdac.in. All such change(s) will automatically become part of this EoI and binding on all applicants. Interested applicants are advised to regularly refer the C-DAC's URLs referred above.
    b. Interested applicants may submit the EoI. C-DAC may ask applicants for clarifications or additional documents at its discretion. Clarifications (if any) will be e-mailed to the applicants.

10 QUALIFICATION CRITERIA

The qualification criteria for the EoI are listed below.

10.1 QUALIFICATION CRITERIA

Sl No	Pre-qualification criteria	Supporting Documents
1.	Applicant shall be a firm / company / partnership firm / trust / society / autonomous body registered under the Companies Act, 2013 / the partnership Act, 1932, Limited Liability Partnership Act, 2008 or any other relevant Law, and who have their registered offices in India.	Copy of certificate of incorporation, registration, partnership deed.
2.	The applicant must have experience in semiconductor packaging, MPW prototyping, and post-silicon validation. Applicant shall detail their experience in other field as well *	Format– 3 Certificate by Authorized Signatory of the applicant or Company Secretary of the firm/organization and other similar documents.
3.	The applicant must not be blacklisted or debarred by any Central Govt. / State Govt. / PSU / Municipal Corporations / other Govt. Bodies, as on date of submission of proposals.	Certificate signed by the Authorized Signatory.
4.	PAN, TAN, GST Registration Certificate.	Copy of Certificate to be enclosed.

Note: * The applicants should provide all the necessary documents as listed in table above. C-DAC reserves the right to reject any proposal not fulfilling the eligibility criteria.

11 EOI EVALUATION

Selection of the successful vendor from the applicants is exclusive prerogative of C-DAC. If the applicant(s) fulfils the eligibility criteria and selected for the above said scope, separate necessary Agreement defining roles and responsibilities of both parties, terms and conditions as to technical, financial, legal aspects etc. will be entered into between the successful vendor and C-DAC.

12 ANNEXURE I

12.1 FORMATS FOR SUBMISSION (FORMAT – 1)

To

The Executive Director

C-DAC, Bangalore

Karnataka – 560038

Subject: Submission of EoI for Delivering Support for Packaging, MPW Prototyping & Post Silicon Validation Services

Dear Sir,

In response to the Invitation for Expression of Interest (EoI) published on C-DAC website for the above purpose, we would like to express interest for the same.

As instructed, we attach all the required documents as specified in EoI document.

1. Application Form (Format - 2)
2. Experience in related fields (Format - 3)
3. Declaration (Format - 4)
4. Format for undertaking with respect to compliance of restrictions for countries which share land border with India as stipulated by govt. of India**.** (Format - 5)

Sincerely Yours,

_____

Signature of the Competent Authority (with date)

_____(full name)

_____(designation)

Stamp & Date

Encl.: As above.

Note; This is to be furnished on the letter head of the organization.

12.2 APPLICATION FORM (FORMAT - 2)

SL No	Organizational Details	
1	Name of the organization / year of establishment	
2	Main areas of work	
3	Type of organization firm / company / partnership firm registered under the Indian Companies Act, 1956 / the partnership Act, 1932 etc.	
4	Whether the Applicant has been blacklisted by any Central Govt. / State Govt. / PSU / Govt. Bodies / Autonomous / Anywhere else? If yes, details thereof.	
5	Address of registered office with telephone no. & fax	
6	Name of the Contact Person with Telephone No, Mobile No, Email Id.	
7	Organization chart	
8	Registration copy with any Govt. / Govt. undertaking Companies (if any)	
9	Accreditation Details ISO / CMM	

Scope of Services			
10	**Packaging Support**	Yes/No If Yes, for each service listed, fill in the relevant **Equipment/ Technology/ Infrastructure** that your company possesses.	
a.	Comprehensive Packaging (Custom package design, QFN, BGA, TSOP, DIP, QFP, SOP, PLCC, Material selection, Packaging process development, etc.)	Yes/No	
b.	Advanced Packaging (2.5D, 3D, WLP, Flip-chip, wire bonding, etc.)	Yes/No	

c.	Die Attach and Bonding Services	Yes/No	
d.	Thermal Management	Yes/No	
e.	Assembly Services	Yes/No	
f.	Environmental Testing	Yes/No	
g.	Package Rework and Repair	Yes/No	
11	**MPW Support**	Yes/ No If Yes, for each service listed, fill in the relevant **Equipment/ Technology/ Infrastructure** that your company possesses.	
a.	Prototype Fabrication	Yes/No	
b.	Design Validation	Yes/No	

c.	Process Customization	Yes/No	
d.	IP Integration	Yes/No	
e.	DFT (Design for Test)	Yes/No	
12	**Post Silicon Validation Support**	Yes/ No If Yes, for each service listed, fill in the relevant **Equipment/ Technology/ Infrastructure** that your company possesses.	
a.	ATE support	Yes/ No	
b.	Bench level validation support	Yes/ No	
c.	Functional Testing	Yes/ No	
d.	Electrical Characterization	Yes/ No	
e.	Thermal Characterization	Yes/ No	
f.	Power Integrity and Noise Testing	Yes/ No	
g.	Reliability Assessment	Yes/ No	

h.	Failure Analysis	Yes/ No	
i.	System-Level Validation support	Yes/ No	
j.	OSAT support	Yes/ No	
k.	Custom Test Development	Yes/ No	
13	**Expression of Interest: Spell out the extent of interest**		

Note :

1. If a particular service is not offered, you may leave the corresponding fields blank.
2. List out if any additional services that you can offer and any other **Equipment/ Technology/ Infrastructure** that your company possesses in the below text box.

Enclose:

1. Copy of Certificate of Incorporation
2. Copy of Article of Association in respect of #3 above.
3. Undertaking in respect of #4 above.
4. Format for undertaking with respect to compliance of restrictions for countries which share land border with India as stipulated by govt. of India**.** (Format - 5)

Signature of the Applicant / Authorized Signatory

_____

(Full name of the Applicant / Authorized Signatory)Stamp & Date

12.3 EXPERIENCE OF THE ORGANIZATION (FORMAT – 3)

ORGANIZATION EXPERIENCE

Experience in providing support to services such as Packaging/ Multi-Project Wafer (MPW) Prototyping/ Post Silicon Validation				
Sl. No.	**Items**	**Vertical /Areaof work**	**Number of assignments during last five (05) years**	**Order Value ofeach assignment in Lakhs of INR *(enclose emai of each order)***
1.	Experience of assignments in relevant areas mentioned above			
2.	Experience in carrying out assignments in relevant areas mentioned above in Government / public sector			

Signature of the Applicant / Authorized Signatory

_____

(Full name of the Applicant / Authorized Signatory)Stamp & Date

12.4 DECLARATION (FORMAT – 4)

DECLARATION

We hereby confirm our interest in ***'Delivering Packaging/ MPW Prototyping/ Post Silicon Validation services'*** as per your EoI. All the information provided herewith is genuine and accurate. We have not been blacklisted by any Central Govt. / State Govt. / PSU / Govt. Bodies / Autonomous / any other competent authority. We hereby confirm that we do not have any animosity/hostile interest against C-DAC.

_____

(Authorized Person's Signature)

Name: _____

Designation: _____

Date of Signature: _____

Stamp & Date

Note: The declaration is to be furnished on the letter head of the organization.

12.5 FORMAT FOR UNDERTAKING WITH RESPECT TO COMPLIANCE OF RESTRICTIONS FOR COUNTRIES WHICH SHARE LAND BORDER WITH INDIA AS STIPULATED BY GOVT. OF INDIA.

(On Company Letter Head, to be signed by the duly authorized person)

Date :
EOI NO. :
TITLE OF EOI :

To,

Centre for Development of Advanced Computing (C-DAC),
A Scientific Society of Ministry of Electronics & Information Technology (MeitY),
Government of India
No.1, Old Madras Road, Byappanahalli,
Bengaluru – 560038

Dear Sir/Madam,

In line with the guidelines issued for compliance of Restrictions for Countries which share land border with India – as issued by Govt. of India in July'2020, I/We have read the clause regarding restrictions on procurements from an applicant of a country which shares a land border with India and on sub-contracting to contractors from such countries.

a. I/We certify that we are not from such a country or if from such a country has been registered with the competent authority. I hereby certify that we fulfil all requirements in this regard and are eligible to be considered.

b. I/We certify that we are not from such a country or if from such a country has been registered with the competent authority and will not sub-contract any work to a contractor from such countries unless such contractor is registered with the competent authority. I hereby certify that we fulfil all requirements in this regard and are eligible to be considered. (Applicable for works involving possibility of sub-contracting)

I/We hereby certify that I/We fulfil all requirements in this regard and am/are eligible to be considered. [Evidence of a valid registration, if any, by the Competent Authority shall be attached]

Name and Signature of the Authorized Signatory.

Check list

Check list for uploading documents on eProcurement Website

Sl.No.	Description
1.	Expression of Interest (FORMAT - 1)
2.	APPLICATION FORM (FORMAT - 2)
3.	EXPERIENCE OF THE ORGANIZATION (FORMAT – 3)
4.	DECLARATION (FORMAT – 4)
5.	Registration copy with any Govt. / Govt. undertaking Companies (if any
6.	FORMAT FOR UNDERTAKING WITH RESPECT TO COMPLIANCE OF RESTRICTIONS FOR COUNTRIES WHICH SHARE LAND BORDER WITH INDIA AS STIPULATED BY GOVT. OF INDIA
7.	The bidder must not be black listed by any Govt. Organizations as on date of Submission of the bids. A certificate or undertaking to this effect must be submitted**.**
8.	Other documents necessary in support of eligibility criteria, product catalogues, brochures etc.
9.	The bidder should provide sufficient documentary evidence to support the eligibility criteria and exemptions mentioned.
10.	Copies of PAN and GST