CORRIGENDUM- I (Technical& Financial)

TENDER NO: **CDACT.PHS.RD.HDG 083D.279.19-20**

Refer C-DAC, Thiruvananthapuram Tender no **CDACT.PHS.RD.HDG 083D.279.19-20** dated 29-10-2019, for THE PROCUREMENT OF EDA TOOLS FOR DIGITAL IC DESIGN & TAPE-OUT IN DEEP SUB MICRON TECHNOLOGY NODES FOR COMPLEX DIGITAL SYSTEM DESIGNS (EDA-ICD). Subsequent to the queries raised during pre-bid conference held on 11.11.2019 (10:00Hrs) at C-DAC, Thiruvananthapuram, this Corrigendum-I (Technical& Financial) is issued for the information of vendors who wish to participate in this invitation to online bids.

Corrigendum-I (Technical& Financial) with the clarifications & response to queries and amendments are appendedherewith

21.11.2019
Thiruvananthapuram

Sd/
The Section Head (Purchase)
C-DAC, Thiruvananthapuram

Technical

Sl. No	Clarifications/Queries/Change requested & Response to clarifications	Amendment in Tender document
1.	**Qns**: Category A-A1 -specification 4 - As it was asked for support for eRM. eRM is proprietary format of Cadence only, no other vendor supports that. We support SV, SVM and OVM which are standard in the industry. Will this be treated as deviation? ***Ans: No, this won't be treated as deviation. The specification 9-A-A1:4 has been amended***	Support for UVM based verification methodologies with optional support for other methodologies such as OVM and eRM.
2.	**Qns**: Category B- B1-Specification 16- Please elaborate this specification. This does not seem like an LEC requirement for LEC function ***Ans: The LEC tool should be capable of handling any customized or complex optimizations carried out by synthesis, place and route tool; if not there should be provision in the LEC tool to provide the attributes/directives to take care of advanced/customized optimizations. The specification 10-B-B1:16 has been amended for clarity***	Support to configure the LEC tool for logic optimization/restructuring which may occur in datapath/clock paths as part of advanced optimization techniques for area and timing.
3.	**Qns:** Category D- D1-Specification 10- Please elaborate this specification-need	Support for Clock Mesh capabilities for clock tree synthesis to achieve low skew and high OCV

	more explanation of this capabilities ***Ans: The specification 12-D-D1:10 has been amended for clarity***	tolerance
4.	**Qns:** Category D- D1-Specification 13- Please elaborate this specification-need more explanation of this capabilities ***Ans: The specification 12-D-D1:13 has been amended for clarity***	Support for concurrent physical and electrical optimization of clock and data paths in the design
5.	**Qns:** Category D- D3-Specification 5- Need more clarity on datapath w.r.t advance node as it in added in this category ***Ans: The specification 12-D-D3:5 has been amended for clarity***	Context-driven placement &Structured datapath support considering advanced node placement & routing requirements
6.	**Qns:** Category G- G1-Specification 8 - IEEE1500 is very old format but instead we support iJTAG1687 -will this be treated as deviation ***Ans: No, this won't be treated as deviation if iJTAG1687 is an IEEE format and a superset of IEEE1500***	Nil
7.	**Qns:** Category G- G1-Specification 11 - Support for Compression features such as OPMISR+. OPMISR+ is Cadence proprietary format. We support other formats so will it be treated as deviation ***Ans: No, this won't be treated as deviation. Its explicitly mentioned in the tender document as "compression features like XOR/OPMISR+/HYBRID" The particular term is mentioned based on previous usage and intended to convey what is intended by Compression features. The vendor can support their own formats to support the functionality of the mentioned format. The specification 15-G-G1:11 has been amended for clarity.***	Support for test compression features to reduce test time and pattern volume without reducing fault coverage figures.
8.	**Qns:** Category G- G1-Specification 15 - On Product clock generation (OPCG) - At speed testing methodology should be supported in Synthesis & Test environment. The term "OPCG" is proprietary.	Support for at speed testing using on-chip PLL

	Ans: If OPCG term is not relevant for a particular vendor, the vendor may only need to comply with the functionality intended by the specification. The specification 15-G-G1:11 has been amended for clarity.	
9.	**Qns**: Please elaborate on License requirement e.g 240 floating license usable for 4 years with user flexibility for start date and end date of each license. ***Ans: The RFP clearly states licenses as "countrywide floating monthly licenses" As per the example quoted, A total number of 240 monthly licenses has to be made available for C-DAC . C-DAC will have the flexibility to choose the start date of each monthly license during the course of 4 years from the date of delivery of the items. C-DAC will have the flexibility to consume each of these monthly licenses any time during a total period of 4 years from the date of delivery of the items.***	Nil
10.	**Qns**: L1 will be decided for complete tender or it is decided based on each category of product. ***Ans: It is explicitly mentioned in clause 5.21 of the RFP that a potential vendor has to support all the categories combinedly*** .	Nil
11.	**Qns:** We have only one part no (or one product) for many specification e.g. C1, C2, C3/D1, D2 and D3- Is it ok if we quote maximum desired quantity for that part no (product) ***Ans: As per the RFP each item mentioned under different 'Categories' are supposed to be independent solutions handled by different design/implementation teams for the execution of the project. Each "Category" will be treated as independent solution and license requirement has to be complied independent of the license requirements of other 'Categories'. "Sub category" can be treated as additional features/options within a single 'Category'***	Nil

	and the bidder need to comply with the required license requirements for enabling the features/ options mentioned in the RFP. As per the examples mentioned in the query C1, C2 and C3 can be one solution and vendor need to quote for the maximum desired quantity to meet the license requirements of C1, C2 and C3. Similarly D1, D2 and D3 can be another solution and vendor need to quote for the maximum desired quantity to meet the license requirements of D1, D2 and D3. But D1, D2 and D3 license requirements should be quoted independent of C1, C2 and C3 license requirements.	
12.	**Qns**: 14 Category F- specification 11 - Typically decoupling cap analysis is supported, no optimization ***Ans: The solution offered should identify the scope of decoupling cap optimization after decoupling cap analysis.***	Nil
13.	**Qns**: 14 Category F- specification 12 - Package model for IR drop analysis is supported. PCB model needs to be handled separately ***Ans: The solution offered should have a well defined methodology for analysing the power based on the considering the PCB parasitic as well.***	Nil
14.	**Qns**: 12 Category D- specification 2 - Silicon Virtual Prototyping: Does this mean a mock-PnR run, then it can be achieved through "ICC2 -feasibility-flow". The floorplan ranking capability is a utility available on SOLVNET. ***Ans: Silicon Virtual Prototyping means mock PnR run to have an initial estimates of the design.***	Nil
15.	**Qns**: Category A-A1 -specification 4 - ERM not supported ***Ans: The specification 9-A-A1:4 has been amended***	Support for UVM based verification methodologies with optional support for other methodologies such as OVM and eRM.
16.	**Qns**: Category A-A1 -specification 11 - Support for unified coverage database	Nil

	integrating simulation, formal, acceleration and use case coverage. Software not supported. ***Ans: The coverage specified is not the coverage of the software code, instead it is the design coverage of the RTL/netlist incorporating the coverage of simulation, formal, acceleration, software/firmware based RTL simulations and use case coverage.***	
17.	**Qns:** Category B- B1-Specification 5 - Should have Semantic and Structural checks capability - What is meant by semantic? ***Ans: Semantic means basic syntax check of the HDL input formats supported***	Nil
18.	**Qns:** Category B- B2-Specification 3 - What is meant by including support for shorts and opens? ***Ans: The solution offered should have a method to flag functional non equivalence arising due to shorts and opens in power and ground connectivity.***	Nil
19.	**Qns:** Category B- B3-Specification 8 - Tool should optimize changes, estimate routing, and legally place the generated ECO logic into the design floor plan, write out the ECO netlist and the corresponding placement DEF file? ***Ans: The solution offered should have a methodology to give an optimized results for the functional ECOs in terms of placement and routing. This can also be achieved by interfacing with other solutions quoted as part of this RFP.*** ***Ans: The specification 10-B-B3:8 has been amended***	Tool should support a well defined methodology to optimize changes, estimate routing, and legally place the generated ECO logic into the design floor plan, write out the ECO netlist and the corresponding placement DEF file.
20.	**Qns:** Should read the DEF layout database corresponding to the original design Netlist, LEF, Liberty Synthesis libraries and SDC to optimally map ECO logic to standard cell and gate-array spare gates mainly for post mask ECO analysis ***Ans: The solution offered should have a***	Should have a well defined methodology to support metal level ECOs considering the existing DEF layout database corresponding to the original design netlist, LEF, Liberty Synthesis Libraries and SDC for post mask ECO.

	methodology to give an optimized results for the functional ECOs in terms of placement and routing. This can also be achieved by interfacing with other solutions quoted as part of this RFP. Post Mask ECO analysis refers to the ECO changes that can occur in selected metal layers after GDSII tape out to the foundry. ***The specification 10-B-B3:9 has been amended***	

Financial

Sl. No	Clarifications/Queries/Change requested & Response to clarifications	Amendment in Tender document
1.	**Qns**: Section clause number as per RFP : 5.26, Request you to amend to waiver off Tender fee & EMD amount against submission of Valid NSIC/MSME registered certificate vendor(valid Documents will attach along with Tender). ***Ans: The clause 5.26 in section 5 has been amended for clarity.***	The Tender Fee and EMD have to be submitted as mentioned below. a. Tender Fee of INR 2,240/- should be submitted as DD. No cost of Tender for documents downloaded by the bidders. b. Bidder can submit Bid Securing Declaration as per the format given in 19.13 of this document or Earnest Money Deposit (EMD) for an amount of INR 24 lakhs through NEFT /Demand Draft (DD)/Bank Guarantee (BG). c. Tender fee and EMD can be waived off for Vendors, registered with MSME / NSIC with valid certificate duly issued by concerned competent authority. d. The pro forma for Bank Guarantee for EMD is as given in section 19.12 Bid Securing Declaration is as given in section 19.13
2.	**Qns**: Can OEM have a commission agent which participates in the open tender with a authorization letter. CDAC will still place PO on OEM and pay OEM, OEM will pay the commission agent their commission. In this case the EMD will be paid by the OEM. Does this work? ***Ans: The clause 8.8 in section 8 has been amended for clarity.***	Terms of payment a. 30% payment of product cost shall be made within 30 days after receipt and acceptance of the ordered items in good conditions of performance standard. b. 60% payment of product cost shall be made after successful completion of installation and training as mentioned under clause 8.7 of General Clauses. c. Balance 10% payment against Performance Bank Guarantee valid for 60 days beyond the validity period of 4 year term based licenses/after 60 days beyond the validity period of 4 year term based licenses. d. Bank charges inside India shall be borne by C-DAC; the contractor shall bear all the bank charges outside India. e. Domestic bidders are required to quote and accept the payment in Indian currency. Similarly Indian agents of foreign suppliers are required to accept their applicable agency commission in Indian currency the equivalent

		thereof shall be adjusted against the payment to the principal; costs for imported goods, may be quoted in any one of the foreign currencies as per BoQ and same shall be paid accordingly in that currency on award of contract.
3.	**Qns**: EMD Amount Rs 24 Lacs. Is it Exempted for MSMEs having UAN No? What Exemption Certificate is needed for waiver of EMD? ***Ans: The clause 5.26 in section 5 has been amended for clarity.***	The Tender Fee and EMD have to be submitted as mentioned below. a. Tender Fee of INR 2,240/- should be submitted as DD. No cost of Tender for documents downloaded by the bidders. b. Bidder can submit Bid Securing Declaration as per the format given in 19.13 of this document or Earnest Money Deposit (EMD) for an amount of INR 24 lakhs through NEFT /Demand Draft (DD)/Bank Guarantee (BG). c. Tender fee and EMD can be waived off for Vendors, registered with MSME / NSIC with valid certificate duly issued by Government of India. d. The pro forma for Bank Guarantee for EMD is as given in section 19.12 Bid Securing Declaration is as given in section 19.13
4.	**Qns**: Section 8.4: Security Deposit (10% of Contract Value) should be submitted within 15 Days. what is its deposit period? ***Ans: The clause 8.4-b clearly stipulates the deposit period as 60 days from the date of award of contract***	Nil
5.	**Qns:** Section 8.6: Performance Bank Guarantee (10% of contract Value) for Period 4 Years 60 Days. When to submit it? ***Ans: As mentioned in clause 8.8:c , upon submission of the performance bank guarantee by the contractor, the balance 10% of payment will be released. Else, the balance 10% payment will be made only after 60 days beyond the validity period of 4 year term based licenses.***	nil
6.	**Qns:** Are PBG (as per section 8.6)and Security deposit (as per section 8.4)same or	Security deposit: a. Within 15 working days of the receipt of

	to be submitted separately ? ***Ans: The clause 8.4 in section 8 has been amended for clarity.***	notification of award of contract from C-DAC(T), the successful Bidder shall furnish interest free Security Deposit in the form of Bank Guarantee, for satisfactory execution of the Contract. b. Security Deposit shall be equal to 10 percent (Ten Percent) of the value of the contract in the form of bank guarantee from a nationalized/scheduled bank valid for 60 days from the date of award of contract. c. Failure of the successful Bidder to submit the Security Deposit within 15 working days shall constitute sufficient grounds for the annulment of the award and execution of the Bid Securing Declaration/forfeiture of the bid security (EMD). d. In the event of non-execution of the Purchase order/Contract or breach of any terms and conditions of the Purchase Order, the Security Deposit shall be forfeited. e. Combined/separate pro forma for Performance Bank Guarantee for contract execution and for warranty execution shall be provided to the contractor on the date of award of contract.
7.	**Qns:** What is Proforma Bank Guarantee as mentioned in Section 19.12. Is it format of Bank Guarantee duly approved by Bank Officials? ***Ans: Section 19.12 is the pro forma Bank guarantee for EMD. The bidder has to follow the given format only if applicable***	Nil
8.	**Qns:** We thank you for kindly answering our queries in today's pre-bid meeting regarding EMD exemption, Security Deposit and PBG. However we have one more query after clarifications on Security deposit and PBG. Please let us know if we as an distributor quote and secure PO, this Security Deposit can be provided by OEM on our behalf. ***Ans: The bank guarantees for Security deposit and PBG should be given with the name of the bidder.***	Nil
9.	Bidder Scenarios - Please confirm if below scenarios are accepted or not	Terms of payment a. 30% payment of product cost shall be made

	a. OEM (foreign vendor) submitting their offer directly in USD and having a technical support presence in India. -OEM foreign office will take the order in USD -India office will provide registration certificate (support office) -Commercial documents like financials and taxation documents will be from OEM foreign office -BG requirements will be taken care by OEM through foreign bank (India office) b. Indian agent will submit the offer and submit all required company financials and tax documents -Request CDAC to place the PO on OEM in USD -All BG requirements will be taken care by Indian agent / by OEM through its bank in India ***Ans : Scenario-'a' : No*** ***Scenario-'b': yes, the Domestic bidders has to quote and accept the payment in Indian currency. Indian agents of foreign suppliers has to accept their agency commission in Indian currency; costs of imported goods, which are directly imported against the contract, can be quoted in any one of the foreign currencies as per BoQ and paid accordingly in that currency. Ans: The clause 8.8 in section 8 has been amended for clarity.***	within 30 days after receipt and acceptance of the ordered items in good conditions of performance standard. b. 60% payment of product cost shall be made after successful completion of installation and training as mentioned under clause 8.7 of General Clauses. c. Balance 10% payment against Performance Bank Guarantee valid for 60 days beyond the validity period of 4 year term based licenses/after 60 days beyond the validity period of 4 year term based licenses. d. Bank charges inside India shall be borne by C-DAC; the contractor shall bear all the bank charges outside India. e. Domestic bidders are required to quote and accept the payment in Indian currency. Similarly Indian agents of foreign suppliers are required to accept their applicable agency commission in Indian currency the equivalent thereof shall be adjusted against the payment to the principal; costs for imported goods, may be quoted in any one of the foreign currencies as per BoQ and same shall be paid accordingly in that currency on award of contract.
10.	**Tender acceptance letter** - Can we add SLMA (License agreement) requirement in this acceptance letter as all our customers need to be complied by our license agreement ***Ans : Yes, But prior to attaching, the SLMA should be submitted to C-DAC and get duly approved by The Section Head (Purchase) , C-DAC. Contractor may add a covering letter to the Tender acceptance letter mentioning about the addition of the approved SLMA.***	Nil
11.	**A.2 Qualification Clause Compliance (QCC)**	Nil

	form: Clause 12 Provide C-DAC the rights to procure each category of tools independent (Can we not comply with this point) ***Ans : The bidder needs to comply with this clause***	
12.	**A.2 Qualification Clause Compliance (QCC) form:** Clause 14 Pre-requisites for bidders on past orders (Request you to relax this point, as just to furnish previous purchase orders from OEM/bidding party for quoted products) ***Ans : Previously executed purchase orders of quoted products from OEM satisfying the order values as mentioned in the RFP are acceptable***	Nil

Tender Clauses

As per the email communication from C-DAC corporate dated 7th November 2019, with reference to order from MeitY ref. no. G-35020/2/2019-Fin.II dated 15th October 2019, clause 2 (d) the tender document is amended to include the option of submitting Bid Securing Declaration in place of Bid Security (Earnest Money Deposit) at the discretion of the vendor. So the following clauses are amended to incorporate the addition.

Section: 4 Prerequisites

Sl. No	Requirements	Documents Required
5	The Bidder shall attach the Tender fee which is non-refundable as mentioned in the section 5.26 of this document. The Bidder can submit Bid Securing Declaration or MSME/NSIC certificate or Earnest Money Deposit (EMD) through NEFT /Demand Draft (DD)/Bank Guarantee (BG) as mentioned in the clause 5.26 of this document.	Bid Securing Declaration/ MSME or NSIC certificate / Unique Transaction Reference Number / Demand Draft / BG

Section: 5 Terms and Conditions

5.26 The Tender Fee and EMD have to be submitted as mentioned below.

a. Tender Fee of INR 2,240/- should be submitted as DD. No cost of Tender for documents downloaded by the bidders.

b. Bidder can submit Bid Securing Declaration as per the format given in 19.13 of this document or Earnest Money Deposit (EMD) for an amount of INR 24 lakhs through NEFT /Demand Draft (DD)/Bank Guarantee (BG).

c. Tender fee and EMD can be waived off for Vendors, registered with MSME / NSIC with valid certificate duly issued by concerned competent authority.

d. The pro forma for
Bank Guarantee for EMD is as given in section 19.12
Bid Securing Declaration is as given in section 19.13

Section: 8 General Clauses

8.4 Security deposit:

a. Within 15 working days of the receipt of notification of award of contract from C-DAC(T), the successful Bidder shall furnish interest free Security Deposit in the form of Bank Guarantee, for satisfactory execution of the Contract.
b. Security Deposit shall be equal to 10 percent (Ten Percent) of the value of the contract in the form of bank guarantee from a nationalized/scheduled bank valid for 60 days from the date of award of contract.
c. Failure of the successful Bidder to submit the Security Deposit within 15 working days shall constitute sufficient grounds for the annulment of the award and execution of the Bid Securing Declaration/forfeiture of the bid security (EMD).
d. In the event of non-execution of the Purchase order/Contract or breach of any terms and conditions of the Purchase Order, the Security Deposit shall be forfeited.
e. Combined/separate pro forma for Performance Bank Guarantee for contract execution and for warranty execution shall be provided to the contractor on the date of award of contract.

8.8 Terms of payment

a. 30% payment of product cost shall be made within 30 days after receipt and acceptance of the ordered items in good conditions of performance standard.
b. 60% payment of product cost shall be made after successful completion of installation and training as mentioned under clause 8.7 of General Clauses.
c. Balance 10% payment against Performance Bank Guarantee valid for 60 days beyond the validity period of 4 year term based licenses/after 60 days beyond the validity period of 4 year term based licenses.
d. Bank charges inside India shall be borne by C-DAC; the contractor shall bear all the bank charges outside India.
e. Domestic bidders are required to quote and accept the payment in Indian currency. Similarly Indian agents of foreign suppliers are required to accept their applicable agency commission in Indian currency the equivalent thereof shall be adjusted against the payment to the principal; costs for imported goods, may be quoted in any one of the foreign currencies as per BoQ and same shall be paid accordingly in that currency on award of contract.

Section: 19 Technical Bid

b. Bid Securing Declaration/EMD/ Exemption certificate for waiver of EMD (refer 19.1)

e. Financial and Undertaking documents

1. BG (refer 19.12)/ Bid Securing Declaration (refer 19.12) company letter head with proper seal and signature of authorized person (with name, designation & contact no.)

19.1 Details of EMD

Earnest Money Deposit Details

Sl. No.	Unique Transaction Reference Number/Demand Draft/ Bank Guarantee no. & date	Amount (INR)	Name of the Bank, Branch, IFSC Code	EMD Waiver (Bid Securing Declaration / MSME or NSIC certificate)
1				

Note:

1. Bid Securing Declaration to be submitted in a separate cover in the Technical bid cover super-scribed with "**Bid Securing Declaration"**
2. MSME/NSIC with valid certificate duly issued by Government of India to be submitted in a separate cover in the Technical bid cover super-scribed with "**MSME/NSIC certificate"**
3. Unique transaction Reference Details, Bank Guarantee, Demand Draft towards EMD and the template containing the EMD details are to be submitted in a separate cover in the Technical bid cover super-scribed with "**Earnest Money Deposit"**

19.13 Pro forma of Bid Securing Declaration

< In Bidders letter head >

Date: [Insert: date of bid]
e-Tender No: CDACT.PHS.RD.HDG 083D.279.19-20

From
(Registered name and address of the bidder)
To:
THE HEAD, PURCHASE SECTION
CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING
VELLAYAMBALAM
THIRUVANANTHAPURAM – 695033

Bid securing undertaking declaration

We, the undersigned on behalf of and under the authority of M/s ……(herein after referred to as bidder) hereby undertakes to declare:

1. That we, the bidder understand that, vide clause 5.26 in section 5 of the RFP cited above , bids can be supported with a Bid Securing Declaration, in lieu of submitting Earnest Money Deposit specified in the said clause as attached at section 9.12 of the said RFP and
2. That we, the bidder understand that, we shall be automatically be suspended from being eligible for bidding in any contract with the Centre for Development of Advanced Computing(C-DAC) (herein after referred to as Purchaser) for a period of 3 years/or for a period as decided by the competent authority, commencing from the closing date of bid submission, on breach, by the bidder, of any of the following obligation(s) under the bid conditions:-
   i. On withdrawal from the proposal or on enhancement of the quoted price subsequent to the bid opening and/or during the Bid validity period or of its extended period, if any.
   ii. On failing to accept and/or execute the contract after being the successful bidder in accordance with the terms and conditions (including timelines for execution of the Agreement) of the said RFP/Purchase Order issued thereof or on failure to furnish the performance security in accordance with the terms and conditions (including timelines for furnishing performance security) of the said RFP/purchase order issued thereof.
   iii. On indulging in any act that would jeopardize or unnecessarily delay the process of bid evaluation/finalization/execution of the proposed contract in accordance with timelines as specified by the purchaser.
3. That we, the Bidder understand that this declaration shall expire on our not being a successful Bidder and on notice of the award of the said contract to another Bidder or thirty days after the validity of the Bid; whichever matures earlier.

(Signature)
Authorized Signatory
Name :
Designation :
Office Seal :
Place :
Date :

20 Price Bid

Commercial Bid shall be submitted online as described in Annexure-B.

1 Commercial Bid covering letter
2 Price bid as per BoQ.xls duly filled

1. Commercial Bid Covering Letter Template

< In Bidders letter head >

Date: [Insert: date of bid]
From
(Registered name and address of the bidder)
To:
THE HEAD, PURCHASE SECTION
CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING
VELLAYAMBALAM
THIRUVANANTHAPURAM – 695033

Dear Sir,
Having examined Tender Document number CDACT.PHS.RD.HDG083D.279.19-20 dated _____ the receipt of which is hereby acknowledged, we, the undersigned, offer supply, installation & commissioning and operationalisation of …… (meaning as realized in Tender Document) at C-DAC, in full conformity with the said Tender Document, for a total project cost of …… (…… only). The above amount is in accordance with the Price Schedules herewith made part of this bid as per the price bid template.

1. We undertake that we shall successfully setup and demonstrate the solution offered to C-DAC in conformity with the bidding documents (and as amended from time to time) for a total cost as provided in the price bid if the contract is awarded to us.

2. We declare that we have studied Tender Document and are making this proposal with a stipulation that you shall award us Contracts, either in part or whole, for the supply, installation, implementation, Integration & commissioning and operationalisation of **EDA TOOLS FOR DIGITAL IC DESIGN & TAPE-OUT (EDA-ICD)** in deep submicron technology nodes for complex digital system designs at C-DAC, identifying separately including all other services specified in the Contract Documents.

3. We have read the provisions of Tender Document and confirm that these are acceptable to us. All necessary clarifications, if any, have been sought for by us and duly clarified in writing, by C-DAC, Thiruvananthapuram. We understand that any other ambiguous clauses in the Tender Document, if any, are subject to interpretation of C-DAC (T).

4. We undertake, if our bid is accepted, to commence the work on the project immediately upon your Notification of Award to us, and to achieve Completion within the time stated in the Bidding Documents.

5. If our bid is accepted, we undertake to execute all contractual documents and provide all securities & guarantees as required in the bid document (and as amended from time to time).

6. We undertake that, in competing for (and, if the award is made to us, in executing) the above contract, we will strictly observe the laws against fraud and corruption in force in India namely "Prevention of Corruption Act".

7. We agree to abide by this bid, consisting of this letter, the tender fee, Bid Securing Declaration, EMD, Technical bid, for a period of bid validity from the date fixed for submission of bids as stipulated in the Tender Document, and it shall remain binding upon us and may be accepted by you at any time before the expiration of that period.

Dated this [insert: number] day of [insert: month], [insert: year] Signed: ……
In the Capacity of [insert: title of position]

Duly authorized to sign this bid for and on behalf of [insert: name of the Bidder]

Witness:
Address:

Annexure-A: MAC and QCC form

A.1 Minimum Acceptance Criteria (MAC) Compliance Form

Sl. No	Requirements	Document Code	Documents Submitted (Y/N)
5	EMD as Unique Transaction Reference Number/DD or BG bank certificate/Bid Securing Declaration/MSME or NSIC certificate submitted	D06	

Annexure-B: Instructions for Online Submission

B.4 Submission of bids:

f. Bidder has to select the payment option as `offline' to pay the tender fee / EMD as applicable and enter details of the instrument(s). Bidder can pay Tender Fee/EMD through NEFT and submit the Unique Transaction Reference Number instead.

Annexure-D: Checklist

Sl. No.	Documents	Y/N
2	Scanned copy of Bid Securing Declaration/Unique Transaction Reference Number/Demand Draft/BG/Exemption Certificate towards Earnest Money Deposit along with EMD details (refer 19.1)	

Annexure-G: Tender Acceptance Letter

6. I / We certify that all information furnished by the our Firm is true & correct and in the event that the information is found to be incorrect/untrue or found violated, then your department/ organization shall without giving any notice or reason therefore or summarily reject the bid or terminate the contract, without prejudice to any other rights or remedy including the execution of Bid Securing Declaration / forfeiture of the full earnest money deposit absolutely.

Centre for Development of Advanced Computing (C-DAC)
A Scientific Society of Ministry of Electronics & IT, Government of India
Vellayambalam, Thiruvananthapuram
Kerala - 695033
Tel: 0471 2723333
www.cdac.in

e-TENDER DOCUMENT

FOR

THE PROCUREMENT OF

EDA TOOLS FOR DIGITAL IC DESIGN & TAPE-OUT

IN DEEP SUB-MICRON TECHNOLOGY NODES FOR COMPLEX DIGITAL SYSTEM DESIGNS

(EDA-ICD)

e-Tender No: CDACT.PHS.RD.HDG 083D.279.19-20
Date: 29.10.2019

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1 Tender Schedule:

Tender Reference number: CDACT.PHS.RD.HDG 083D.279.19-20

1	Name and Address of the Purchaser	The Section Head (Purchase) Centre for Development of Advanced Computing, P B No 6520, Vellayambalam, Thiruvananthapuram - 695033, Kerala Phone: +91 471 2723333, 2312627 Fax : +91 471 2723456 email: purchase-tvm@cdac.in
2	Closing Time and Date for receipt of online bids	On or before 17:00 hours of 13-12-2019.
3	Name of the Contact Person for any clarification	The Section Head (Purchase) Centre for Development of Advanced Computing, P B No 6520, Vellayambalam, Thiruvananthapuram - 695033, Kerala Phone: +91 471 2723333, 2312627 Fax : +91 471 2723456 email: purchase-tvm@cdac.in
4	Validity of the Bid	120 days from the date of opening of Technical Bid

Activity	Date
Release/Issue of Tender Document	29.10.2019 (17:00Hrs)
Last date for submission of written queries for clarifications on Tender document	05.11.2019 (10:00Hrs)
Pre-Bid Conference (Venue: C-DAC, Thiruvananthapuram)	11.11.2019 (10:00Hrs)
Last date for submission of written queries for clarifications on Tender document raised during pre-bid conference	15.11.2019 (11:00Hrs)
Last date for reply to written queries of prospective bidders	21.11.2019 (17:00 Hrs)
Start date and time of submission of Bids	28.11.2019 (09:00 Hrs)
Last date & time of submission of Bids	13.12.2019 (17:00 Hrs)
Opening of Technical Bids	16.12.2019 (15:00 Hrs)
Opening of Financial Bids	Will be informed later

2 Introduction

Centre for Development of Advanced Computing (C-DAC) is a Scientific Society under the Ministry of Electronics & Information Technology (MeitY), Government of India. One of the thrust areas of C-DAC is VLSI & Embedded system design involving complex FPGA implementations, Million gate ASIC designs in deep submicron, Analog and Mixed Signal Design and Embedded System development.

This e-Tender is for the procurement of **EDA TOOLS FOR DIGITAL IC DESIGN & TAPE-OUT (EDA-ICD)** in deep submicron technology nodes for complex digital system designs. The EDA-ICD solution should broadly support the entire RTL to GDSII flow requirements in 14nm such as RTL Verification, Logic Equivalence Checking, RTL Synthesis, Floorplanning, Partitioning, Place & Route, Signoff Timing analysis, Signoff power analysis, DFT & ATPG, Extraction & Physical verification etc.

Interested Bidders are advised to study this Tender document carefully before submitting their bids. Submission of a bid in response to this Tender shall be deemed to have been done after careful study and examination of this document with full understanding of Prerequisites, Terms & Conditions and Implications.

Any bid received by C-DAC after the deadline will be summarily rejected. C-DAC shall not be responsible for any delay in submission and no further correspondence on the subject will be entertained. For any clarification on Tender, please contact Section Head (Purchase), C-DAC, Thiruvananthapuram.

The Tender document contains specifications under eight categories, viz. Category-A: Verification Solution; Category-B: Logic Equivalence Checking Solution; Category-C: RTL Synthesis Solution; Category-D: Floorplanning, Partitioning, Place & Route Solution, Category-E: Signoff Timing Solution; Category-F: Signoff Power Solution; Category-G: DFT & ATPG Solution; Category-H: Extraction & Physical Verification Solution.

To consider a bid, the Minimum Acceptance Criteria (MAC) and Qualification Clause Criteria (QCC) should be met and a Certificate of Compliance, as per the attached MAC and QCC format, duly signed by Company's Authorized person should be submitted. The prospective bidder should meet all the clauses mentioned under the Minimum Acceptance Criteria (MAC) & Qualification Clause Criteria (QCC), Prerequisites and Terms & Conditions.

Bidders have to submit their bids in two bid format,

Bid 1: Technical bid
Bid 2: Price bid

on or before the due date and time specified.

A Technical bid will be considered only if the bidder explicitly meets all the clauses mentioned in the MAC & QCC forms, Prerequisites and Terms & Conditions. To qualify the "Technical" bid, all the "Functions" mentioned in each Subcategory under the respective Category has to be explicitly met.

The "Price bid" will be considered only if the "Technical Evaluation" is qualified. The Price Bid should be as per the given format (BoQ.xls).

3 Minimum Acceptance Criteria & Qualification Clause Criteria

The attached Minimum Acceptance Criteria (MAC) compliance format and Qualification Clause Criteria (QCC) compliance format (Annexure-A) should be submitted in Company's Letter head duly signed by Company's Authorized person.

Any bid, not meeting any one of the qualification requirements & clauses mentioned under MAC & QCC (Annexure-A), Prerequisites and Terms & Conditions will not be considered, and their bids will get rejected summarily.

4 Prerequisites

Sl. No	Requirements	Documents Required
1	The Bidder should be a legally valid registered entity in India since last 3 years. The Bidder should have been in operation in India for a period of at least 3 years.	a. Certificate of Incorporation. b. Annual Reports for the last 3 years.
2	In case the bidder being an OEM company, the Authorized Signatory signing the Bid on behalf of the OEM company should be duly authorized by the OEM Company to sign the Bid and the Agreement on their behalf.	A Certificate from the OEM Company board on their letter head with a reference number and date certifying that the Bid signatory is authorized by the Company to do so.
3	In case of bidder being an Agent signing the Bid on behalf of the OEM supplier, the bidder should be duly authorized by the OEM Company to sign the Bid and the Agreement on their behalf.	A Certificate from the OEM Company, on their letter head having reference number and date, certifying that the agent is authorized to Bid on their behalf and the signatory is authorized by the Company to do so.
4	As on date of submission of the proposal, the bidder and the OEM company shall not be under any declaration of ineligibility for unsatisfactory past performance, corrupt or fraudulent practices, any other unethical business practices or blacklisted either by Ministry/Department of Government of India/State Governments.	Certificate from the Company authorized signatory to the effect that the bidder and the OEM company are not blacklisted by any of the Ministry/ Department of Government of India/ State Governments.
5	The Bidder shall attach the Tender	

	fee which is non-refundable as mentioned in the section 5.26 of this document. The Bidder can submit Bid Securing Declaration or MSME/NSIC certificate or Earnest Money Deposit (EMD) through NEFT /Demand Draft (DD)/Bank Guarantee (BG) as mentioned in the clause 5.26 of this document.	Bid Securing Declaration/ MSME or NSIC certificate / Unique Transaction Reference Number / Demand Draft / BG
6	The Bidder shall submit IT PAN,TAN and GST document with relevant certificates as applicable.	a. Copy of PAN b. Copy of TAN c. Copy of GST Document
7	Average Annual turnover for the last three financial years (April-March) not less than Rs.3 crores, ending 31st March 2019.	Signed and Scanned copies of a. Financial performance for last three years as per Financial Information format specified in Annexure-E b. Audited Annual accounts / balance sheet along with Profit & Loss account for the financial year 2016-17, 2017-18 and 2018-19.
8	Bid validity	120 days from the date of opening of Technical Bid

5 Terms and Conditions

5.1 The Bidder should submit the bids through e-procurement portal https://eprocure.gov.in/ complete in all respects with technical specifications, including pamphlets and catalogues. Refer Annexure-B for instructions for online submission of the Bid.

5.2 The offer should be valid for a minimum period of 120 days from the date of opening of the Technical Bid.

5.3 The bids can be submitted only as single party for all the categories combinedly and consortium of bidders shall not be entertained.

5.4 Bids will not be entertained after the due date and time.

5.5 Any taxes or statutory levies payable should be shown separately; otherwise quoted price will be treated as all inclusive.

5.6 Any deviation from C-DAC's specification of items shall be clearly indicated in technical bid itself. However, C-DAC reserves all the rights to accept or reject the proposed solution without assigning any reason whatsoever thereof.

5.7 Offers made by Indian Agents on behalf of their Principals, should be supported by the necessary authorization letter from their Principals.

5.8 The Authorization of person submitting the tender, if called for, shall be produced.

5.9 All documents/correspondence should be in English Language only.

5.10 The Purchaser reserves the right to accept or reject the lowest or any other offer in whole or in part without assigning any reason.

5.11 The acceptance of the stores contracted for, is subject to final approval in writing by the Purchaser.

5.12 C-DAC reserves the right to change the quantity of items to be procured or place Purchase Order for selected items only.

5.13 The financial bid should be strictly as per format given in BoQ.xls

5.14 Part shipment of items under each category is not allowed unless specifically agreed to, by C-DAC.

5.15 Where Installation or assembly or commissioning is a part of the contract, it should be done immediately on notification. The Contractor shall be responsible for any loss / damages sustained due to delay in fulfilling this responsibility.

5.16 Bidder shall quote in INR or foreign currency. Exchange rates as of financial bid opening date will be applicable for bid evaluation.

5.17 LD Clause:

The items must be delivered by the contractor according to the Purchase Order. In case of any change, the contractor should inform C-DAC in advance and obtain C-DAC's approval for the revised delivery schedule. If the contractor fails to deliver the entire item or part thereof as per the agreed delivery schedule, C-DAC shall be entitled at its option to recover from the contractor as agreed, Liquidated damages at a sum equivalent to 0.5% of the value of the Items not supplied in time for every week of delay or part of a week thereof subject to a maximum of 10% of order value or to terminate the order.

5.18 Amendment to the Bid Document:

At any time prior to the last time and date for opening of bids, C-DAC, may, for any reason, whether at its own initiative or in response to a clarification requested by a prospective Bidder, modify the Bid Document by an amendment. The amendment will be notified in the e-Procurement website, which will be binding on all bidders. In order to provide prospective Bidders reasonable time in which to take the amendment into account in preparing their bids, C-DAC may, at its discretion, extend the last date for the receipt of Bids.

5.19 The bidder should comply with all Government (State & Central) statutory requirements as per law.

5.20 Jurisdiction:

The disputes, legal matters, court matters, if any shall be subject to Thiruvananthapuram, Kerala jurisdiction only.

5.21 The tender requirements mentioned under each category, viz. Category-A, Category-B, Category-C, Category-D, Category-E, Category-F, Category-G and Category-H shall be treated combinedly and C-DAC shall award the contract only to a single vendor who can support the all specifications mentioned under each category based on recommendations made by Technical and Commercial Evaluation Committees.

5.22 The Items mentioned under each Category should support seamless transition between the solutions offered. So a potential bidder has to bid for all the mentioned categories in total.

5.23 If any of the above terms is not agreeable to the bidder, it should be specifically mentioned in the bid along with the alternative suggested. C-DAC reserves all the rights to accept or reject the suggestion without assigning any reason whatsoever thereof.

5.24 Bids should clearly specify item/equipment delivery and implementation schedule.

5.25 Bidder should ensure that the quoted items are not declared "End of support/maintenance" for the next five years from the date of submission of the bid.

5.26 The Tender Fee and EMD have to be submitted as mentioned below.

a. Tender Fee of INR 2,240/- should be submitted as DD. No cost of Tender for documents downloaded by the bidders.

b. Bidder can submit Bid Securing Declaration as per the format given in 19.13 of this document or Earnest Money Deposit (EMD) for an amount of INR 24 lakhs through NEFT /Demand Draft (DD)/Bank Guarantee (BG).

c. Tender fee and EMD can be waived off for Vendors, registered with MSME / NSIC with valid certificate duly issued by concerned competent authority.

d. The pro forma for

Bank Guarantee for EMD is as given in section 19.12

Bid Securing Declaration is as given in section 19.13

6 Instructions to Bidder

6.1 A Pre-bid conference shall be held with the prospective bidder as per schedule given in the Tender document at C-DAC, Thiruvananthapuram, India to clarify issues regarding the specifications and other details of the procurement.

The prospective bidder must, therefore, ensure that they or their authorized representatives attend the said pre-bid meeting at C-DAC as per the given schedule. In order to enable meaningful discussions in the Pre-bid conference, the prospective bidders are requested to list the queries/clarifications planned to be sought by them on this Tender in the Pre-bid conference, in a Query Sheet and send the said Query Sheet in advance to reach C-DAC Thiruvananthapuram as per schedule given in this Tender document before the Pre-bid Conference.

Bidder to intimate their willingness to attend the Pre-bid conference well in advance along with name and designation of person attending (valid passport & visa details in case of foreign nationals) etc. for arranging their entry pass.

In the event where the bidder is unable to attend the Pre-Bid Conference physically, a Pre-Bid Conference through Video Conference/Skype/Conference Call shall be arranged by C-DAC upon request from the bidder(s).

6.2 Request for extension of the due date will not be considered.

6.3 In this tender either the Indian Agent on behalf of the Principal/OEM or the Principal/OEM itself can bid, but both cannot bid simultaneously for the same item. Indian agents while quoting on behalf of their principals shall provide necessary latest authorization letter obtained from their Principals/ Manufacturers in their bid.

6.4 If an agent submits a bid on behalf of the Principal/OEM, the same agent shall not submit a bid on behalf of another Principal/OEM in the tender for the same item. If submitted, all offers submitted by the said agent shall be excluded from the procurement process.

6.5 The tender of bidder who has not agreed to furnish Security Deposit or Performance Bank Guarantee as sought vide this tender shall be excluded from the procurement process.

6.6 Bids with validity period shorter than that specified in the tender enquiry shall be excluded from the procurement process.

6.7 Late bids, fax quotations and e-mail quotations will not be considered.

6.8 C-DAC reserves the right to verify all claims made by the bidder.

6.9 C-DAC reserves the right to change any milestone date of the tendering activity/ tender schedule.

6.10 Bid which is not submitted as per the instructions mentioned herein is liable to be rejected.

6.11 If tender opening date happens to be a public holiday, tender will be opened on the next working day and interested bidder may depute their representatives to attend the Tender Opening, with proper authorization.

6.12 C-DAC shall be under no obligation to accept the lowest or any bid and reserves the right of acceptance of the whole or any part of the bid or portions of the quantity offered and the bidder shall supply the same at the rates quoted.

6.13 C-DAC reserves the right to accept or reject any/or all the bids in part or full without assigning any reasons thereof.

6.14 It is expressly agreed that the acceptance of the Stores Contracted for is subject to final approval in writing by the Purchaser.

6.15 It is to be noted that the drawings, specifications, end-use etc., given by the purchaser, are confidential and shall not be disclosed to any third party.

6.16 Prices are required to be quoted according to the units indicated in the tender. When quotations are given in terms of units other than those specified in the tender form, relationship between the two sets of units must be furnished.

6.17 The quote should indicate quantity wise unit rate separately which have to be filled online as per the price bid template (BoQ.xls). The Prices are to be mentioned both in figures as well as in words. The taxes, duties, levies etc. are to be calculated and indicated in the column provided in online forms explicitly.

6.18 Bidder is expected to comply with commercial and other terms and conditions given in General Clauses of this tender.

6.19 All available technical literature, catalogues and other data in support of the specifications and details of the items should be furnished along with the offer.

6.20 Evaluation license, if called for, should be submitted free of all charges by the bidder and the Purchaser shall not be responsible for any loss or damage thereof due to any reason whatsoever.

6.21 Specifications: Stores offered should strictly conform to C-DAC specifications. Deviations, if any, should be clearly indicated by the bidder in his bid. The bidder should also indicate the Make/Type number of the stores offered and provide catalogues, technical literature and samples, wherever necessary, along with the quotations. Test Certificates, wherever necessary, should be forwarded along with supplies. Wherever options have been called for in our specifications, the bidder should address all such options. Wherever specifically mentioned by C-DAC, the bidder could suggest changes to specifications with appropriate response for the same.

6.22 The Purchaser reserves the right to place order on the successful bidder for additional quantities up to 100% of the quantity offered by them at the rates quoted within six months.

6.23 Subletting and Assignment: The contractor/bidder cannot sublet, transfer or assign the order/Contract or any part thereof or interests therein or benefit or advantage thereof in any manner whatsoever, to any other party without the previous written consent of the purchaser. Such consent by the purchaser, however, shall not relieve or discharge the contractor/bidder from any obligation, duty or responsibility under the Purchase Order/ Contract.

6.24 This being a two part bid, Technical bid and Price bid part separate, the Technical part should not contain Pricing information of the tendered stores. The bids containing Price details of the tendered stores in Technical part will be treated as unsolicited offers and rejected.

6.25 The bids shall be opened as per schedule indicated in the Tender in the presence of the Bidder/their authorized representatives who may like to attend the tender opening against presentation of Authorization letter.

6.26 While submitting the tender documents, bidder should stamp the documents mentioned in Minimum Acceptance Criteria (MAC) with the respective document codes provided in Annexure-A (A.1).

7 Tender Evaluation Criteria:

7.1 Evaluation of Technical Bids:

The following shall be considered for evaluation of Technical Bid:

a. Bidders meeting the MAC, QCC, Prerequisites, Terms & Conditions will be shortlisted and considered as potential bidders.
b. Potential bidders are further subjected to technical scrutiny and evaluation by an expert Technical Evaluation Committee (TEC) for each category.
c. The technical specification compliance and technical evaluation compliance of each potential bidder will be finalized by the respective Technical Evaluation Committee.
d. The technical evaluation for each category will be carried out as mentioned in Annexure-C. The technical qualification of a particular bidder is entirely within the discretion of the respective Technical Evaluation Committee.
e. Only those bidders who are recommended by the respective Technical Evaluation Committee (TEC) will be considered as technically qualified. Price bids from technically qualified bidders will only be considered.
f. The choice of a particular potential bidder as technically qualified will be only based on the recommendations made by TEC.

7.2 Evaluation of Price Bids:

The following shall be considered for evaluation of Price Bid:

a. Price quoted for Category-A, Category-B, Category-C, Category-D, Category-E, Category-F, Category-G and Category-H will be evaluated combinedly by an expert Commercial Evaluation Committee (CEC).
b. Price quoted by the bidder in the price bid template for meeting the functionalities given in the Specification Compliance Form and Technical Evaluation Compliance Form.
c. Compliance with the C-DAC Payment Terms prescribed in this tender document.
d. The choice of a particular technically qualified bidder as Contractor will be only based on the recommendation of CEC.

8 General Clauses

8.1 Definitions:

a. The term Purchaser shall mean Head Purchase, C-DAC, Thiruvananthapuram or his successors or assignees.

b. The term Contractor shall mean, the person, firm or company with whom or with which the order for the supply of stores is placed and shall be deemed to include the Contractor's Successors, representatives, heirs, executors and administrators unless excluded by the Contract.

c. The term Purchase Order shall mean the communication signed on behalf of the Purchaser by an officer duly authorized intimating the acceptance on behalf of the Purchaser of the terms and conditions mentioned or referred to in the said communication accepting the Tender or offer of the Contractor for supply of stores of plant, machinery, Software or equipment or part thereof.

d. The term Stores shall mean all that the Contractor agrees to supply under the Contract as specified in the Purchase Order including its installation, testing and commissioning as per the specifications.

e. The term Technical Evaluation Committee (TEC) shall mean the expert team who will explicitly scrutinize the technical compliance of the prospective bidders against the respective specification compliance requirements, technically evaluating the offered solution against the requirements in technical evaluation compliance form and finalize the technically qualified bidders.

f. The term Commercial Evaluation Committee (CEC) shall mean the expert team who will explicitly scrutinize and evaluate the price bids of the technically qualified bidders and finalize the Contractor for the tender.

8.2 For imported materials, the Purchaser is entitled to issue Customs duty exemption certificate (CDEC) to the contractor under customs notification no.51/96 dated 23.07.1996 and subsequent amendments to enable the contractor to avail of the benefit of concessional rate of customs duty under this notification. In addition to the above CDEC, any documentary support requested by the contractor from the purchaser for customs clearance of goods against the above CDEC shall be provided by the purchaser.

8.3 Prices: Bidders offering firm prices will be preferred.

8.4 Security deposit:

a. Within 15 working days of the receipt of notification of award of contract from C-DAC(T), the successful Bidder shall furnish interest free Security Deposit in the form of Bank Guarantee, for satisfactory execution of the Contract.

b. Security Deposit shall be equal to 10 percent (Ten Percent) of the value of the contract in the form of bank guarantee from a nationalized/scheduled bank valid for 60 days from the date of award of contract.

c. Failure of the successful Bidder to submit the Security Deposit within 15 working days shall constitute sufficient grounds for the annulment of the award and execution of the Bid Securing Declaration/forfeiture of the bid security (EMD).
d. In the event of non-execution of the Purchase order/Contract or breach of any terms and conditions of the Purchase Order, the Security Deposit shall be forfeited.
e. Combined/separate pro forma for Performance Bank Guarantee for contract execution and for warranty execution shall be provided to the contractor on the date of award of contract.

8.5 Delivery period:

The bidder shall deliver all items in BoQ (Annexure-F) within 30 days from the date of award of contract.

8.6 Updates and maintenance:

a. The Contractor must provide free technical support including software updates, maintenance releases and bug fixing for the entire Annual Maintenance Contract (AMC) period from the date of acceptance at C-DAC.
b. The Contractor must also quote separately for AMC per perpetual license including technical support, maintenance releases and bug fixing for three subsequent years from the end of first year from the date of acceptance at C-DAC on company letter head from an authorized signatory.
c. Performance Bank Guarantee: To fulfill conditions of 4 year time based license requirements, the Contractor shall furnish a Bank Guarantee (as per format given by purchaser) from any nationalized/scheduled bank for an amount equivalent to 10 percent of the value of the Contract and shall be valid for 60 days beyond the validity period of 4 year term based licenses.
d. On performance and completion of the Contract in all respects, the Bank Guarantee will be returned to the Contractor without any interest.

8.7 Installation and training:

a. Installation as per Purchasers tendered specifications shall be carried out by the Contractor at C-DAC, Thiruvananthapuram at no extra cost to the purchaser. The contractor shall provide in advance guidelines for preparation of the installation site and list of items to be supplied by the Purchaser during installation. On receipt of intimation from the Purchaser, the Contractor shall depute its engineer(s) to the Purchasers site to carry out installation and will demonstrate the functionality of the tendered stores to Purchasers specifications as per the Scope of Installation given in Technical specification sheet within 10 days from the date of delivery. The Contractor shall be responsible for any loss/damages sustained due to delay on the part of the Contactor to send its engineer for installation.
b. Training: Contractor shall provide an initial detailed training to the concerned C-DAC personnel on all the functionalities as mentioned in the Specification of EDA TOOLS FOR DIGITAL IC DESIGN & TAPE-OUT (EDA-ICD) in deep submicron technology nodes for complex digital system designs.

8.8 Terms of payment

a. 30% payment of product cost shall be made within 30 days after receipt and acceptance of the ordered items in good conditions of performance standard.
b. 60% payment of product cost shall be made after successful completion of installation and training as mentioned under clause 8.7 of General Clauses.
c. Balance 10% payment against Performance Bank Guarantee valid for 60 days beyond the validity period of 4 year term based licenses/after 60 days beyond the validity period of 4 year term based licenses.
d. Bank charges inside India shall be borne by C-DAC; the contractor shall bear all the bank charges outside India.
e. Domestic bidders are required to quote and accept the payment in Indian currency. Similarly Indian agents of foreign suppliers are required to accept their applicable agency commission in Indian currency the equivalent thereof shall be adjusted against the payment to the principal; costs for imported goods, may be quoted in any one of the foreign currencies as per BoQ and same shall be paid accordingly in that currency on award of contract.

8.9 Validity:

The Bid must be valid for a minimum period of 120 days from the date of opening of Technical Bid.

The Bid with validity period shorter than the period specified in the tender document shall be excluded from the procurement process.

8.10 Guaranteed time delivery:

The time for and the date of completion of the entire work stipulated in the Purchase Order shall be deemed to be the essence of the Contract. The purchase order must be executed within the date specified therein.

8.11 Contractors default liability:

The purchaser may upon written notice of default to the Contractor terminate the Contract in whole or in part in circumstances detailed hereunder:

a. If in the judgment of the Purchaser, the Contractor fails to make delivery of Stores within the time specified in the Contract/ agreement or within the period for which extension has been granted by the Purchaser to the Contractor.
b. If in the judgment of the Purchaser, the Contractor fails to comply with any of the other provisions of this Contract.

8.12 Replacement:

If the stores or any portion thereof is damaged or lost during transit, the Purchaser shall give notice to the Contractor setting forth particulars of such stores damaged or lost during transit. The replacement of such stores shall be effected by the Contractor within a reasonable time to avoid unnecessary delay in the intended usage of the Stores.

8.13 Rejection:

In the event that any of the stores supplied by the Contractor is found defective in material or workmanship or otherwise not in conformity with the

requirements of the Contract specifications, the purchaser shall either reject the stores or request the Contractor, in writing, to rectify the same. The Contractor, on receipt of such notification, shall either rectify or replace the defective stores free of cost to the purchaser. If the Contractor fails to do so, the purchaser may at his option either:

a. replace or rectify such defective stores and recover the extra cost so involved from the Contractor, or
b. terminate the Contract for default as provided under clause 8.11 (General Clauses)

8.14 Extension of time:

If the completion of supply of stores is delayed due to reason of force majeure such as acts of God, acts of public enemy, acts of Government, fires, floods, epidemics, quarantine restriction, strikes, freight embargoes, etc., the Contractor shall give notice within 15 days to the purchaser in writing of his claim for an extension of time. The purchaser on receipt of such notice after verification, if necessary, may agree to extend the Contract delivery date as may be reasonable but without prejudice to other terms and conditions of the Contract.

8.15 Arbitration:

If at any time any question, dispute or difference whatsoever shall arise between the purchaser and the Contractor upon or in connection with this Contract, either party may forthwith give to the other notice in writing of the existence of such question, dispute or difference and the same shall be referred to the adjudication of two arbitrators, one to be nominated by purchaser, other by a Contractor and in the event of any difference of opinion, the arbitrators will refer the matter to the umpire. The arbitration shall be conducted in accordance with the rules and procedure for arbitration of the International Chamber of Commerce at Paris. The expenses of the arbitrators and umpire shall be paid as may be determined by them. However, the venue of such arbitration should be in India.

In case a dispute arises with domestic/Indian suppliers, the applicable Arbitration procedure shall be as per Indian Arbitration & Conciliation Act, 1996.

8.16 Indemnity:

The Contractor shall warrant and be deemed to have warranted that all Stores supplied against this Contract are free and clean of infringement of any patent, copyright or trade mark and shall at all times indemnify the purchaser against all claims which may be made in respect of stores for infringement of any right protected by Patent, Registration of design or Trade Mark and shall take all risk of accident or damage which may cause a failure of the supply from whatever cause arising and the entire responsibility for the sufficiency of all the means used by him for the fulfillment of the Contract.

8.17 Counter terms and conditions of suppliers:

Where counter terms and conditions/printed or cyclostyled conditions have been offered by the supplier, the same shall not be deemed to have been

accepted by the purchaser unless specific written acceptance thereof is obtained.

8.18 Applicable law:

The Contract shall be interpreted, construed and governed by the laws of India.

9 Category-A: Specification of Verification Solution

Sl. No.	Specifications
Sub Category -A1: Logic Simulation Tool	
1	Should support languages -Verilog (IEEE 1364), SystemVerilog (IEEE 1800) including SVA, VHDL (IEEE 1076) and SystemC (IEEE 1666)
2	Simulation execution should support four-state logic (0, 1, X, Z) in all modes
3	Simulator should have waveform window, register window, unified transaction/signal viewing, schematic viewing etc
4	Support for UVM based verification methodologies with optional support for other methodologies such as OVM and eRM
5	Support for low power, X-propagation, and mixed signal simulation
6	Support for unified debug for all use cases including interactive and batch debug
7	Support for standard debug tools including direct dump of waveforms
8	Support for zero delay and unit delay gate level simulation to resolve race and loop conditions
9	Lint checking support to analyse synthesizability ,race condition, code reusability, clock domain, synchronization, fsm coding checks
10	Support for gate-level netlist analysis for any DFT errors introduced during synthesis
11	Support for unified coverage database integrating simulation, formal, acceleration, software and use case coverage
12	Support for functional coverage analysis using PSL, SVA, and OVL assertion constructs.
13	Should support coverage attributes like blocks, paths, expressions, variables, gates, FSM (states,sequences), and toggle and should provide bitwise expression scoring
14	Support for Automatic finite state machine extraction
15	Support for multi-threading on multi-core processors/distributed processing over network/ CPU acceleration for faster verification turnaround time
Sub Category -A2: Low power support	
1	Logic simulation tool should support low-power simulation using IEEE 1801.
2	Simulator support for verification of shutoff and restore behavior at the design level, for the logical netlist, and through to physical implementation
3	The simulator should have support to measure coverage on low-power objects, power-modes, and power-states
Sub Category -A3: Formal Verification	
1	Formal proof based verification of SVA properties for Verilog /VHDL based designs
2	GUI support for asserion visualization, filtering, grouping etc.
3	Support for complex datapath verification such as DSP, Processor Pipeline, FPU units etc.
4	Support for formal property checks for LINT such as range overflows, artihmetic overflows, X-assignments, simultaneous set/reset, full case, parallel case, bus contention etc.
5	Support for X-propagation verification and analysis
6	Support for formal based sequential equivalence checks to ensure the functionality after incorporating low power optimization techniques, performance optimization techniques etc.

7	Support for connectivity checks along with debugging, schematic viewing, source code browsing capabilities
8	Support for formal scoreboarding enabling data integrity verification of data path designs
9	Support for sign-off quality property verification with formal coverage analysis capabilties to identify unreachable points
10	Support for strong interactive UI & Debug environment with in-line value annotation, on the fly assertion and constraint editing capabilities
11	Support for control and status register checks by generating properties to capture register interaction, latency, read/write semantics etc.

10 Category-B: Specification of Logic Equivalence Checking Solution

Sl. No.	Specifications
Sub Category -B1: Logic Equivalence Checks	
1	Support for VHDL 1987, VHDL1993, VHDL2008, Verilog 1995, Verilog 2001, System Verilog 1800-2009 HDL input formats
2	Support for Dual language equivalence checking
3	Support to verify multi-million–gate designs without using test vectors
4	Support RTL vs Netlist and Netlist vs Netlist checks
5	Should have Semantic and Structural checks capability
6	Should have Complex datapath equivalence checking capability
7	Should be Technology independent
8	Graphical User Interface (GUI) for debugging and automatic error checking with following feature support ❖ Schematic viewer that shows logic values for each vector ❖ Full cross-highlight in between RTL model and circuit ❖ Logic-cone pruning to focus debugging on relevant information
9	Support for flat datapath module verification
10	Should have Carry-save verification capability
11	Should support entire verification at various stages from from RTL to final layout
12	Should support scan chains
13	Support for pipeline retimed equivalence checks
14	Support for advanced pipeline check and diagnosis
15	Support for Hierarchical equivalence checking
16	Support to configure the LEC tool for logic optimization/restructuring which may occur in datapath/clock paths as part of advanced optimization techniques for area and timing
17	Should be capable of generating the analysis report for design
18	Complex Datapath optimization verification Support
19	Provision for functionality comparison between SPICE netlist created for LVS or extracted from GDS to the RTL or gate model

Sub Category-B2: Low Power Logic Equivalence Checks	
1	Should supports multisupply voltage (MSV) islands, coarse grain power gating (PSO), coarse-grain ground switching (GSO), dynamic voltage and frequency scaling (DVFS), and state retention power gating design techniques
2	Low Power LEC support for PSW, isolation, level shifting, and state retention
3	Should report ❖ Incorrect power and ground connectivity, including shorts and opens ❖ Instances with undefined power domains or mixed power domains ❖ Missing, redundant, and incorrect power connection and wrong level shifter types ❖ Missing, redundant, and incorrect isolation cell power connectivity ❖ Power control signals to power switches, isolation cells, and state retention registers that are not powered ❖ Incorrect power connection to state retention registers
Sub Category-B3: Logic Equivalence Check ECO flow	
1	Tool should combine logic equivalence checking with functional ECO analysis, design Netlist modification, and logic optimization
2	Should handle both small and large complex ECOs in batch mode
3	Should be independent verification tool
4	Should have ECO analysis engine that can identify the differences between the original design netlist and the new design Netlist
5	User should be able to perform ECO analysis on the entire design or on specific modules within the design hierarchy
6	Once the ECO analysis step is completed and the logic change optimized, tool should perform the necessary Netlist modification to achieve the new function in the original design Netlist
7	Should write out an ECO script that can be used to make direct changes to the place-and-route database
8	Tool should support a well defined methodology to optimize changes, estimate routing, and legally place the generated ECO logic into the design floor plan, write out the ECO netlist and the corresponding placement DEF file.
9	Should have a well defined methodology to support metal level ECOs considering the existing DEF layout database corresponding to the original design netlist, LEF, Liberty Synthesis Libraries and SDC for post mask ECO.
10	Should have graphical debugging via an integrated schematic viewer that shows logic values for each error vector
11	Should have Full cross-highlighting between RTL model and circuit
12	Logic-cone pruning to focus debugging on relevant information
13	Automatic error candidate identification

11 Category-C: Specification of RTL Synthesis Solution

Sl. No.	Specifications
Sub Category-C1: RTL Synthesis	
1	Support for VHDL 1987, VHDL1993, VHDL2008, Verilog 1995, Verilog 2001, System Verilog 1800-2009 HDL input formats
2	Support for SDC based design constraints and TcL based command reference flow.
3	Support for Hierarchical/Flat HDL designs of gate sizes ≥ 75Million gate instances
4	Extensive flexibility for users to control optimization on specific areas of designs
5	Provision to generate TcL backend tool scripts to achieve better QoR based on synthesis constraints/optimization directives
6	Provision to generate TcL based scripts for Industry Standard Logic Equivalence Checking tool and Test Insertion tools for seamless transition of the design between various design tools to achieve better QoR based on synthesis constraints/optimization directives
7	Support for Integrated Static Timing Analyzer with automatic extraction, analysis of full timing and physical contexts of any block/module/subset of a design
8	Provision for seamless integration of synthesizer output files into Industry standard Sign off Timing/Power Analysis tools
9	Cross-probing between HDL, schematic and Industry standard timing & power reports/database with GUI support
10	Support for Pipeline and general register retiming
11	Support for Designware/Chipware/Similar <Vendor>ware functional components and simulation models
12	Support for entire design DFT logic insertion and optimization
13	Support for Concurrent Multimode Multi Corner timing analysis and optimization
14	Support for Advanced datapath/Arithmetic optimization techniques for better QoR based on the required user application
15	Ability to re-synthesize, restructure and optimize the critical path on an incremental basis at various stages of RTL to Gate level conversion
16	Ability to support automatic mapping of the complex library elements present in the technology library for better QoR along with extensive flexibility for users to control the complex cell insertion and QoR analysis
17	Support for multi-threading on multi-core processors/distributed processing over network/ CPU acceleration for faster synthesis turnaroundtime (Default base license should support at least 8 CPU cores and option to increase more with additional CPU acceleration licenses)
Sub Category-C2: Physically Aware Synthesis	
1	Physically aware logic structure and mapping with results correlation within 5 -10% of physical implementation
2	Should perform global synthesis optimization using real physical wire delay
3	Should eliminate the need to add excessive timing margin during synthesis, enabling further power and area reduction

4	Should present physical feedback to logic designer to help drive corrective action during synthesis
5	Should support Native congestion modeling to enable automatic congestion optimization, analysis and fixing.
6	Morphing and Demorphing for congestion optimization
7	Congestion aware DFT logic placement
8	Should support Top down register retiming balance logic across the registers, maximizing the data throughput in single-pass synthesis run
9	Should support Physical aware clock gating
10	Should support Physical aware logic structuring on congested SOC, improves total negative slack , area , wire length & power
11	Should support Physical aware mapping to improve worst negative slack, total negative slack and congestion
12	Physical Multibit inferencing to improve the leakage power
13	Should support Physical aware Engineering Change Order (ECO)
14	Should support Physical aware DFT synthesis
Sub Category-C3: Low Power Synthesis	
1	IEEE 1801 based low power design flow
2	Multi-Vt insertion/optimization based on design constraints and optimization directives
3	Hierarchical RTL Clock gating, operand isolation, DVFS, Power Shut-off etc
4	Automatic power domain aware insertion of level shifters, isolation cells, retention elements and Header/Footer switches
5	Always on buffering and power domain aware routing

12 Category-D: Specification of Floorplanning, Partitioning, Place and Route solution

Sl. No.	Specifications
Sub Category-D1: Floorplanning, Place and Route	
1	Support for Hierarchical/Flat HDL designs of gate sizes ≥ 75Million gate instances, exclusive of hard macros
2	Support for ❖ Silicon virtual prototyping ❖ Interactive & Automatic design Floorplanning ❖ Physical synthesis ❖ Design partitioning, pin assignment & timing budgeting ❖ Legal macro & standard cell placement ❖ Power grid design & optimization ❖ Hierarchical CTS ❖ Feed-through insertion, pipeline registers, clock planning
3	Support for automatic floor plan generation for optimal timing, power, area and congestion results with floor plan ranking capabilities
4	Support for Congestion, Timing and power-driven logic re-synthesis & placement

5	Support for tight timing correlation between Synthesis and placement
6	Support for concurrent clock and data optimization
7	Support for bottom-up, top-down hierarchical methodologies with black box modeling support
8	Support for concurrent macro and standard cell placement
9	GUI support for timing, power and clock debug & diagnostics
10	Support for Clock Mesh capabilities for clock tree synthesis to achieve low skew and high OCV tolerance
11	Support for slack driven placement
12	Support for flip-chip RDL routing capabilities
13	Support for concurrent physical and electrical optimization of clock and data paths in the design
14	Support for automatic congestion resolving capabilities and pin access by intelligent placement/spacing of standard cells
15	Support for vector/vectorless based dynamic and leakage power optimization
16	Support for optimal routing convergence on timing, area, power, signal integrity and manufacturing goals
17	Support for concurrent Via pillar optimization and enhancement
18	Support for tight correlation between pre-route and post route analysis
19	Support for Multi Mode Multi Corner analysis of the design
20	Support for Multi Corner Clock Tree synthesis
21	Support for ECO at RTL and Netlist level
22	Support to map/place/route ECO cells without affecting QoR
23	Support for Master clone in place optimization
24	Support for IR drop aware placement and power integrity in the flow
25	Support for parallel bus routing, 3D shielding, length matching, differential pair routing and resistance matching
26	Support for all industry standard input and output formats for following
27	GUI support for the entire place and route flow from netlist to GDSII
28	Support for machine learning for better QoR
29	Distributed multi-CPU and multithreaded processing for maximum hardware utilization (Default base license should support at least 8 CPU cores and option to increase more with additional CPU acceleration licenses)
Sub Category-D2: Low Power Support	
1	IEEE 1801 support
2	End-to-end multi-supply voltage (MSV) support
3	Power domain-aware automatic floor plan synthesis
4	Power domain-aware routing
5	Dynamic Voltage Frequency Scaling support (DVFS)
6	Power shut-off and power switch prototyping
7	State Retention Power Gating support
8	Always-on buffer support

9	Hierarchical Macro Model support
Sub Category-D3 : Advance node features	
1	32/28/20/16/14nm support in routing and verify
2	Fully certified down to 14nm at leading foundries
3	FinFet Support - Support for color aware routing for timing improvement in lower technology nodes
4	DPT conflict and DRC check features
5	Context-driven placement &Structured datapath support considering advanced node placement & routing requirements
6	DFM/DFY optimization for wires, cell, vias
7	Critical area for yield analysis
8	Litho-aware routing with prevention and fixing
9	1-D routing support
10	Clock mesh & hybrid implementation

13 Category-E: Specification of Signoff Timing solution

Sl. No.	Specifications
1	Fully certified down to 14nm at leading foundries
2	Concurrent multi-mode and multi corner support
3	Integration with Power Sign off engine for running IR aware STA
4	Support for placement aware timing analysis - timing analysis considering location and length of a path being analyzed
5	Support signoff-accurate and physically aware timing ECO
6	Support for integrated parasitic extraction and power analysis functionality
7	Support for interactive cross-probing functionality
8	Support for overlap and crosstalk effects to ensure proper signal integrity
9	Support for OCV & AOCV to reduce unwarranted pessimism caused by on-chip variation
10	Support for statistical static timing analysis by considering logic correlation between signals
11	Analyze a part of a design independent of the whole design without losing QOR
12	Ability to analyze and report false violations
13	Availability of reference flow or example designs (14nm node preferred)
14	Global timing debug to accelerate root-cause and bottleneck analysis
15	Physically aware engineering change order (ECO) optimization for MMMC
16	MMMC-aware timing debug for quick timing issue identification across all views
17	MMMC signoff ECO optimization and repair across all timing views for fewer ECO cycles. The Physical Aware capability of the tool should allow a signoff timing closure in about 2-3 ECO cycles
18	Distributed multi-CPU and multithreaded processing for maximum hardware utilization (Default base license should support at least 8 CPU cores and option to extend on additional CPU's with additional CPU acceleration licensing)

14 Category-F: Specification of Signoff Power solution

Sl. No.	Specifications
1	Fully certified down to 14nm at leading foundries
2	Calculation and analysis of power consumption, including leakage, internal, and switching power
3	Calculation of vector/vector-less leakage and dynamic power analysis
4	Calculate peak and average power
5	Analyze the design for low power
6	Analysis of the full-chip resistance network, including effective and least resistance
7	Create physical-aware power-density vector profiles
8	Analyze and optimize EM and IR drop effects
9	Carry out hybrid, mixed-mode analysis in the combination of gate/RTL vectors and vector-less
10	Vector-based analysis, including gate/RTL-level VCD/FSDB, test scan-mode, etc.
11	Perform De-coupling cap analysis and optimization
12	Analysis of the impact of power on design closure, from chip to package and PCB
13	Should support industry-standard NLDM and CCS Power libraries
14	Supports voltage and temperature scaling to create unique PVT points from a restricted library
15	Simultaneous and complete analysis of all cross-domain paths under all scenarios
16	Calculate block level power analysis
17	Static Early Rail Analysis using power grid views
18	Support for Chip-package models
19	What-If analysis for static power & power rail R
20	Tight integration with Digital implementation and STA engine
21	Interactive reports & plots
22	Dynamic IR drop and EM analysis
23	Vector-driven & vector less dynamic power & power distribution calculation
24	Dynamic Early Rail Analysis using power grid views
25	Analysis of de-coupling capacitance & rush-current
26	What-If analysis dynamic power, power rail RC, de-coupling capacitance
27	Integration with STA engine for running IR aware STA
28	Missing via checks on Power Network Optimization
29	Clock tree power estimation
30	Distributed multi-CPU and multithreaded processing for maximum hardware utilization (Default base license should support at least 16 CPU cores without additional licensing)

15 Category-G: Specification of DFT & ATPG solution

Sl. No.	Specifications
Sub Category-G1 : DFT	
1	Foundry support down to 14nm
2	Support for full and partial scan insertion
3	Support for timing aware test point insertion
4	Support for physically aware scan-chain stitching
5	Support for power aware timing pattern generation
6	Provide automatic timing constraints for DFT-related paths for faster timing closure
7	Should have Advanced DFT rule checking, Tristate rules , shift register rules , clock rule , async reset/set violation, abstract segment violation
8	IEEE1500 core wrapping methodology for big SOCs
9	Boundary scans (IEEE1149.1 & IEEE1149.6) insertion for digital and analog IOs
10	Test Point analysis and optimization (RRFA/DFA) deterministic fault analysis and random resistance fault analysis for better ATPG patterns and coverage
11	Support for test compression features to reduce test time and pattern volume without reducing fault coverage figures
12	Should support Smart Scan multi-site test, Low power Multi-segment scan. Smart scan is low pin count testing which helps to test multiple devices
13	Smart scan compression with serializer/de-serializer logic in built to achieve low pin count compression
14	Low Pin count test
15	Support for at speed testing using on-chip PLL
16	Power aware test access mechanism with IEEE 1801 to enable the testing of the low power structures in design and generation of the ATPG based on power modes in design
17	Should have single pass fully integrated DFT flow in synthesis
Sub Category-G2 : ATPG	
1	Should support Static test for Full scan, partial scan and sequential ATPG for edge-triggered and LSSD design
2	Integrated test pattern generation for Static, IDDQ, and I/O parametric fault models
3	Support for Timed (SDC and SDF) delay, small delay, and physically aware bridge fault models
4	Should support Core-based testing, test data migration and test reuse
5	Special support for custom designs such as data pipelines, scan control pipelines, and scan safe to insert lock-up latches for a skew safe scan design
6	Net bridging feature - Potential bridge candidate based on net adjacency to be modeled as bridging faults
7	Should support ATPG with power targets during scan and capture events of ATPG
8	Support pattern generation for RAM sequential test
9	Low-power ATPG with scan and capture toggle count limits

10	Distributed CPU support for parallel processing of ATPG
11	Support for user defined fault model at primitive cell, hierarchical block or cell instance levels
12	GUI with interactive analysis capabilities like scan chain tracing and the test coverage analysis
Sub Category-G3 : MBIST	
1	Unified Programmable MBIST engine with programmable capabilities; User programmable algorithms test time applied and modified through the TAP
2	Flexibility for PMBIST logic sharing
3	Verilog testbench generation for validation in a Verilog simulator
4	Support for embedded SRAMs, ROMs, Register Files, unrestricted multiple ports
5	Flexible MBIST interface: Direct Access and JTAG
6	Rich predefined hardcoded memory test algorithms
7	Supports Diagnostics, redundancy repair analysis
8	Support for Soft Repair and interface to hard repair solutions using soft repair interface
9	Support top bottom and bottom up MBIST design insertion flows
10	Flexible scheduling (test plan) of MBIST engines
Sub Category-G4 : LBIST	
11	LBIST with test point insertion for coverage for automotive and defense devices
12	Direct access Logic BIST, JTAG controlled Logic BIST with hierarchical LBIST solution
13	Clock staggering in LBIST mode for reducing the power during LBIST scan mode
14	Lowest area overhead
15	LBIST running at input oscillator frequency
16	Ability to test the LBIST Macro; support for asynchronous set and reset clock testing.
17	Full automated solution with logic synthesis
18	Netlist insertion, connectivity, verification and signature generation

16 Category-H: Specification of Extraction & Physical Verification Solution

Sl. No.	Specifications
Sub Category-H1 : RC Extraction	
1	Support for Black-box, gray-box, or white-box extraction modes
2	Lumped R only, C only, or RC for all nets
3	Coupled C for all nets
4	Self (L) and mutual (K) inductance extraction
5	Fully-distributed RC and RLCK for all nets
6	RLCK for selected nets and C for the rest, or vice versa
7	Hierarchical transistor-level RC extraction
8	Ability to exclude nets, such as power and ground nets
9	Critical net and critical path extraction
10	Supports both transistor-level and cell-level extractions during design implementation and signoff.

11	Integrates seamlessly with both Analog custom design and digital implementation platforms for better productivity enhancement
12	Unlimited Transistor support- There should be no limitation of licensing for design size
13	Unlimited Cell Instances Support-There should be no limitation of licensing for design size
14	Hierarchical Transistor support - There should be no limitation of licensing for design hierarchy. Same license supports flat & hierarchical design extraction
15	Wire Edge Enlargement support
16	Separate bias for Capacitance and Resistance
17	Virtual Metal Fill option
18	Temperature dependent Resistance extraction option
19	Thickness (density) support- For lower node designs (65 & below) dielectric and metal thickness effects to be considered in extraction
20	Multiple Process Corners support
21	Thickness f(d, w) support- For lower node designs (65 & below) dielectric and metal thickness effects to be considered in extraction
22	Field Solver (transistor & cell) support for most accurate capacitance extraction
23	Inductance extraction at cell level
24	Substrate Extraction (RC extraction)
25	Via Effect Extraction
26	Loading Effect Extraction
27	Contact Bias 2D Table (Po-Co spacing, Co-Co spacing)
28	Advanced Modeling features (40nm to 14nm)
29	Multiple retargeting tables support (28, 22nm)
30	Coplanar Metal capacitance support
31	Via Temp dependent temperature coefficient f(area)
32	Slot Vis support
33	Flexible Cap & Res modeling
34	OPC-WEE support
35	2-bias contact support and Contact Dual Bias support
36	All advanced node modelling effects support for FinFet technologies up to 16FF to be supported
37	Certified at all leading foundries for all the nodes up to 16FF
38	Distributed Processing support
39	Multi CPU support for acceleration
Sub Category-H2 : DRC Verification	
1	Should be foundry qualified and certified DRC solution at leading foundries across the process technologies, specially at advanced nodes from 28nm to 14nm
2	Should enable DRC, Antenna, XOR, Fast XOR and Fill capabilities- Fast XOR is for GDS vs. GDS compare
3	Signoff DRC check based on foundry rules
4	Support complex rules checking

5	Integration within Analog Layout, Digital Implementation environments
6	Ability to read/write presets for different form values in GUI- Auto form filling with default values
7	Support limited area checks, by coordinates
8	Support configuration of custom rules
9	Support DRC checks on GDS, Open Access, OASIS formats
10	GUI and command line support
11	Support distributed processing and multi-threading
12	Support DRC on Original Layers, Derived Layers
13	Support grouping of rules by rules
14	Support conditional checks
15	Support select/unselect checks by DRC rules
16	Support reporting of results in different formats i.e. GDS, ASCII, OASIS, OA format
17	Support flat/hierarchical DRC run
18	Support 32/64 bit processing
19	Option to provide maximum number of errors in report
20	Highlight errors in different colors
21	Should allow debugging of results while DRC is running - As DRC is still running, the completed DRC results should be viewed and start fixing the layout.
22	Ability to exclude cells during DRC run
23	Ability to show flat/hierarchical counts of DRC errors
24	Support for LELE/SADP, DPT, TPT, QPT
25	Support for Loop detect, 3D IC, advanced Metal Fill,
26	Support for DFM fill, Track based Fill,
27	Support for Voltage Dependent Rules, FinFet
Sub Category-H3 : LVS Verification	
1	Should be foundry qualified and certified LVS solution at leading foundries across the process technologies, specially at advanced nodes from 28nm to 14nm
2	Enable Layout vs Schematic checks
3	Compare GDSII to Netlist, Netlist to netlist
4	Support 32/64 bit processing
5	Support distributed processing
6	Integration within Analog, Digital design environments
7	GUI and command line support
8	Support GDSII, OASIS, DFII as layout source
9	Support CDL/Spice/Verilog inputs as schematic source
10	Support for power/ground connections on leaf cells
11	Flat and hierarchical run capabilities
12	Support extraction of layout Netlist from GDSII, Layout
13	Ability to create ASCII database for connectivity extraction
14	Support creation of single netlist from different input formats (CDL/Spice/Verilog)

15	Option to provide maximum number of errors in report
16	Ability to create summary/report in detailed format- format for summary/report is Text (All reports) , ASCII, GDS, OASIS (ERC – Electrical rule check reports)
17	Support identification for Soft Check errors
18	Support virtual connect rules for unconnected nets
19	Support identification of opens/Shorts
20	Support identification of Power/Ground shorts
21	Support reporting of Malformed devices
22	Support recognition of gates i.e. simple and all
23	Support auto match capability for automatic matching- matching of cell names in layout & schematic
24	Support hcells to be defined during LVS for name mismatch in source and layout
25	Support automatic generation of hcells
26	Support definitions of Power/Ground net names for extraction
27	Ability to ignore port names during comparison
28	Support filtering of devices from netlist based on device connectivity
29	Support definition of black box cells
30	Support for Stamping Conflict Debug
31	Graphical LVS debus support
32	FinFET parameter genFIN, LDE support
33	Device signature support
34	3D IC (LVS related) support
35	Advanced device parameter support

17 Terms for Installation, Training and Licensing

Sl. No.	Specifications
1	Installation and provide complete training, tutorials at C-DAC, Thiruvananthapuram
2	Full flow has to be provided by the single bidder for better integration and application support across the project
3	Vendor has to provide additional trainings and tool related flow support during the AMC period as requested by C-DAC
4	Vendor should be able to accommodate any change in license quantities (between purchased products not exceeding the overall cost)
5	Vendor has to submit relevant foundry signoff certifications and customer success references flow using the tool chains quoted at advanced node up to 14nm
6	Training and tutorials should cover all design, functional, feature aspects of the offered solution and should be provided directly by the application engineers from OEM
7	The offered solution must be tested for all the specifications prior to installation/ delivery
8	Operating System: Linux/Unix

9	**Licensing Scheme for Category-A: Verification Solution**	
	Sub Category -A1: Logic Simulation Tool	
	1	240 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	8 countrywide floating perpetual licenses inclusive of 1 year AMC
	Sub Category -A2: Low power support	
	1	12 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	1 countrywide floating perpetual licenses inclusive of 1 year AMC
	Sub Category -A3: Formal Verification	
	1	1 countrywide floating perpetual licenses inclusive of 1 year AMC
10	**Licensing Scheme for Category-B:Logic Equivalence Checking Solution**	
	Sub Category -B1: Logic Equivalence Checks	
	1	72 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC
	Sub Category-B2: Low Power Logic Equivalence Checks	
	1	12 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	1 countrywide floating perpetual licenses inclusive of 1 year AMC
	Sub Category-B3: Logic Equivalence Check ECO flow	
	1	12 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	1 countrywide floating perpetual licenses inclusive of 1 year AMC
11	**Licensing Scheme for Category-C: RTL Synthesis Solution**	
	Sub Category -C1: RTL Synthesis	
	1	48 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	3 countrywide floating perpetual licenses inclusive of 1 year AMC
	Sub Category-C2: Physically Aware Synthesis	
	1	48 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	3 countrywide floating perpetual licenses inclusive of 1 year AMC
	Sub Category-C3: Low Power Synthesis	
	1	12 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	1 countrywide floating perpetual licenses inclusive of 1 year AMC

12	**Licensing Scheme for Category-D:Floorplanning, Partitioning Place & Route Solution:**	
	Sub Category-D1: Floorplanning, Place and Route	
	1	84 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	4 countrywide floating perpetual licenses inclusive of 1 year AMC
	Sub Category-D2: Low Power Support	
	1	12 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	1 countrywide floating perpetual licenses inclusive of 1 year AMC
	Sub Category-D3 : Advance node features	
	1	42 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC
13	**Licensing Scheme for Category-E: Signoff Timing Solution:**	
	1	84 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	4 countrywide floating perpetual licenses inclusive of 1 year AMC
14	**Licensing Scheme for Category-F: Signoff Power Solution:**	
	1	42 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC
15	**Licensing Scheme for Category-G: DFT & ATPG Solution:**	
	Sub Category-G1 : DFT	
	1	12 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC
	Sub Category-G2 : ATPG	
	1	12 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC
	Sub Category-G3 : MBIST	
	1	6 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	1 countrywide floating perpetual licenses inclusive of 1 year AMC
	Sub Category-G4 : LBIST	
	1	6 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	1 countrywide floating perpetual licenses inclusive of 1 year AMC

16	**Licensing Scheme for Category-H: Extraction & Physical Verification Solution:**	
	Sub Category-H1 : RC Extraction	
	1	72 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC
	Sub Category-H2 : DRC Verification	
	1	72 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC
	Sub Category-H3 : LVS Verification	
	1	72 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC

18 Terms for Customer Support

Sl. No.	Specifications
1	Support should be provided by the respective OEMs of each items directly. C-DAC should be able to raise the support queries with the OEM Field application engineers directly through email or online support portals.
2	Full technical support with complete documentation/white papers and video tutorials. Support should be provided through Email/Fax/support system and depending on the gravity of the problem, Field Application engineer shall visit C-DAC for solution of problem on mutually agreeable basis.
3	OEM shall carry out any number of emergency visits during warranty and AMC period as and when required. The maximum response time from OEM must not be more than 48 hours (excluding holiday).
4	All expenses on the visit(s) of the OEM's engineer such as to and fro travel costs, local transportation, boarding and lodging etc. during warranty and AMC period shall be borne by the OEM/Contractor.
5	OEM should regularly provide & install upgrades, updates, service packs, patches of the Software Products, released during the warranty period, even if the existing capabilities of the licensed software are enhanced / released with a different brand name/trade mark.
6	C-DAC should be provided with the online on-demand tutorials, study materials, documents, databases, advanced online learning courses available as part of the training material for the entire solution offered against each of the specification during the entire AMC period
7	Since the purchase is primarily intended for a mission critical project, in addition to the regular support services provided by the OEM, a one point contact window should be assigned for C-DAC for the entire AMC period by OEM who is well versed in RTL to GDSII design & tape out technology nodes up to 14nm.

19 Technical Bid

Technical Bid comprising of the following shall be submitted as described in Annexure-B

a. Tender fee

b. Bid Securing Declaration/EMD/ Exemption certificate for waiver of EMD (refer 19.1)

c. Pre-qualification criteria supporting documents (refer Annexure-A)

d. Technical Compliance and Support documents:

1. Specifications compliance form: Verification solution (refer 19.2)
2. Specifications compliance form: Logic Equivalence Checking Solution (refer 19.3)
3. Specifications compliance form: RTL Synthesis Solution (refer 19.4)
4. Specifications compliance form: Floorplanning, Partitioning, Place& Route Solution (refer19.5)
5. Specifications compliance form: Signoff Timing solution (refer 19.6)
6. Specifications compliance form: Signoff Power solution (refer 19.7)
7. Specifications compliance form: DFT & ATPG solution (refer 19.8)
8. Specifications compliance form: Extraction & Physical Verification solution (refer 19.9)
9. Terms compliance: Installation, Training and Licensing (refer 19.10)
10. Terms compliance: Customer Support (refer 19.11)
11. Technical support documents (Brochures, data sheets etc)

e. Financial and Undertaking documents

1. BG (refer 19.12)/ Bid Securing Declaration (refer 19.13) company letter head with proper seal and signature of authorized person (with name, designation & contact no.)
2. Financial Information on company letter head with proper seal and signature of authorized person (with name, designation & contact no.) (refer Annexure-E)
3. An authorization letter issued by the competent authority on company letter head authorizing the signatory to sign on behalf of the bidder.
4. Undertaking to the effect that the terms and conditions, clauses etc. stipulated under section 5 of this Tender document with proper seal and signature of authorized person (with name, designation & contact no.).
5. Undertaking to the effect that the terms and conditions, clauses etc. stipulated under section 8 of this Tender document with proper seal and signature of authorized person (with name, designation & contact no.).
6. A scanned copy of the commercial bid without prices (**prices blocked**) with acceptance to commercial terms & conditions with proper seal and signature of authorized person (with name, designation & contact no.) (refer Section 20).
7. Tender Acceptance Letter on company letter head with proper seal and signature of authorized person (with name, designation & contact no.) (refer Annexure-G)
8. Signed copy of the downloaded Tender document

19.1 Details of EMD

Earnest Money Deposit Details

Sl. No.	Unique Transaction Reference Number/Demand Draft/ Bank Guarantee no. & date	Amount (INR)	Name of the Bank, Branch, IFSC Code	EMD Waiver (Bid Securing Declaration / MSME or NSIC certificate)
1				

Note:

1. Bid Securing Declaration to be submitted in a separate cover in the Technical bid cover super-scribed with "**Bid Securing Declaration"**
2. MSME/NSIC with valid certificate duly issued by Government of India to be submitted in a separate cover in the Technical bid cover super-scribed with "**MSME/NSIC certificate"**
3. Unique transaction Reference Details, Bank Guarantee, Demand Draft towards EMD and the template containing the EMD details are to be submitted in a separate cover in the Technical bid cover super-scribed with "**Earnest Money Deposit"**

19.2 Specifications compliance form: Verification Solution

Sl. No.	Specifications	Compliance (Yes/No)	Remarks
Sub Category -A1: Logic Simulation Tool			
1	Should support languages -Verilog (IEEE 1364), SystemVerilog (IEEE 1800) including SVA, VHDL (IEEE 1076) and SystemC (IEEE 1666)		
2	Simulation execution should support four-state logic (0, 1, X, Z) in all modes		
3	Simulator should have waveform window, register window, unified transaction/signal viewing, schematic viewing etc		
4	Support for UVM based verification methodologies with optional support for other methodologies such as OVM and eRM		
5	Support for low power, X-propagation, and mixed signal simulation		
6	Support for unified debug for all use cases including interactive and batch debug		
7	Support for standard debug tools including direct dump of waveforms		
8	Support for zero delay and unit delay gate level simulation to resolve race and loop conditions		
9	Lint checking support to analyse synthesizability ,race condition, code reusability, clock domain, synchronization, fsm coding checks		
10	Support for gate-level netlist analysis for any DFT errors introduced during synthesis		
11	Support for unified coverage database integrating simulation, formal, acceleration, software and use case coverage		
12	Support for functional coverage analysis using PSL, SVA, and OVL assertion constructs.		
13	Should support coverage attributes like blocks, paths, expressions, variables, gates, FSM (states,sequences), and toggle and should provide bitwise expression scoring		
14	Support for Automatic finite state machine extraction		
15	Support for multi-threading on multi-core processors/distributed processing over network/ CPU acceleration for faster verification		

	turnaround time		
Sub Category -A2: Low power support			
1	Logic simulation tool should support low-power simulation using IEEE 1801.		
2	Simulator support for verification of shutoff and restore behavior at the design level, for the logical netlist, and through to physical implementation		
3	The simulator should have support to measure coverage on low-power objects, power-modes, and power-states		
Sub Category -A3: Formal Verification Tool			
1	Formal proof based verification of SVA properties for Verilog /VHDL based designs		
2	GUI support for asserion visualization, filtering, grouping etc.		
3	Support for complex datapath verification such as DSP, Processor Pipeline, FPU units etc.		
4	Support for formal property checks for LINT such as range overflows, artihmetic overflows, X-assignments, simultaneous set/reset, full case, parallel case, bus contention etc.		
5	Support for X-propagation verification and analysis		
6	Support for formal based sequential equivalence checks to ensure the functionality after incorporating low power optimization techniques, performance optimization techniques etc.		
7	Support for connectivity checks along with debugging, schematic viewing, source code browsing capabilities		
8	Support for formal scoreboarding enabling data integrity verification of data path designs		
9	Support for sign-off quality property verification with formal coverage analysis capabilties to identify unreachable points		
10	Support for strong interactive UI & Debug environment with in-line value annotation, on the fly assertion and constraint editing capabilities		
11	Support for control and status register checks by generating properties to capture register		

	interaction, latency, read/write semantics etc.		

19.3 Specifications compliance form: Logic Equivalence Checking Solution

Sl. No.	Specifications	Compliance (Yes/No)	Remarks
Sub Category -B1: Logic Equivalence Checks			
1	Support for VHDL 1987, VHDL1993, VHDL2008, Verilog 1995, Verilog 2001, System Verilog 1800-2009 HDL input formats		
2	Support for Dual language equivalence checking		
3	Support to verify multi-million–gate designs without using test vectors		
4	Support RTL vs Netlist and Netlist vs Netlist checks		
5	Should have Semantic and Structural checks capability		
6	Should have Complex datapath equivalence checking capability		
7	Should be Technology independent		
8	Graphical User Interface (GUI) for debugging and automatic error checking with following feature support ❖ Schematic viewer that shows logic values for each vector ❖ Full cross-highlight in between RTL model and circuit ❖ Logic-cone pruning to focus debugging on relevant information		
9	Support for flat datapath module verification		
10	Should have Carry-save verification capability		
11	Should support entire verification at various stages from from RTL to final layout		
12	Should support scan chains		
13	Support for pipeline retimed equivalence checks		
14	Support for advanced pipeline check and diagnosis		
15	Support for Hierarchical equivalence checking		
16	Support to configure the LEC tool for logic optimization/restructuring which may occur in datapath/clock paths as part of advanced optimization techniques for area and timing		
17	Should be capable of generating the analysis report for design		

18	Complex Datapath optimization verification Support		
19	Provision for functionality comparison between SPICE netlist created for LVS or extracted from GDS to the RTL or gate model		
Sub Category-B2: Low Power Logic Equivalence Checks			
1	Should supports multisupply voltage (MSV) islands, coarse grain power gating (PSO), coarse-grain ground switching (GSO), dynamic voltage and frequency scaling (DVFS), and state retention power gating design techniques		
2	Low Power LEC support for PSW, isolation, level shifting, and state retention		
3	Should report ❖ Incorrect power and ground connectivity, including shorts and opens ❖ Instances with undefined power domains or mixed power domains ❖ Missing, redundant, and incorrect power connection and wrong level shifter types ❖ Missing, redundant, and incorrect isolation cell power connectivity ❖ Power control signals to power switches, isolation cells, and state retention registers that are not powered ❖ Incorrect power connection to state retention registers		
Sub Category-B3: Logic Equivalence Check ECO flow			
1	Tool should combine logic equivalence checking with functional ECO analysis, design Netlist modification, and logic optimization		
2	Should handle both small and large complex ECOs in batch mode		
3	Should be independent verification tool		
4	Should have ECO analysis engine that can identify the differences between the original design netlist and the new design Netlist		
5	User should be able to perform ECO analysis on the entire design or on specific modules within the design hierarchy		
6	Once the ECO analysis step is completed and the logic change optimized, tool should perform the necessary Netlist modification to achieve the new		

	function in the original design Netlist		
7	Should write out an ECO script that can be used to make direct changes to the place-and-route database		
8	Tool should support a well defined methodology to optimize changes, estimate routing, and legally place the generated ECO logic into the design floor plan, write out the ECO netlist and the corresponding placement DEF file.		
9	Should have a well defined methodology to support metal level ECOs considering the existing DEF layout database corresponding to the original design netlist, LEF, Liberty Synthesis Libraries and SDC for post mask ECO.		
10	Should have graphical debugging via an integrated schematic viewer that shows logic values for each error vector		
11	Should have Full cross-highlighting between RTL model and circuit		
12	Logic-cone pruning to focus debugging on relevant information		
13	Automatic error candidate identification		

19.4 Specifications compliance form: RTL Synthesis Solution

Sl. No.	Specifications	Compliance (Yes/No)	Remarks
Sub Category-C1: RTL Synthesis			
1	Support for VHDL 1987, VHDL1993, VHDL2008, Verilog 1995, Verilog 2001, System Verilog 1800-2009 HDL input formats		
2	Support for SDC based design constraints and TcL based command reference flow.		
3	Support for Hierarchical/Flat HDL designs of gate sizes ≥ 75Million gate instances		
4	Extensive flexibility for users to control optimization on specific areas of designs		
5	Provision to generate TcL backend tool scripts to achieve better QoR based on synthesis constraints/optimization directives		
6	Provision to generate TcL based scripts for Industry Standard Logic Equivalence Checking tool and Test Insertion tools for seamless transition of		

	the design between various design tools to achieve better QoR based on synthesis constraints/optimization directives		
7	Support for Integrated Static Timing Analyzer with automatic extraction, analysis of full timing and physical contexts of any block/module/subset of a design		
8	Provision for seamless integration of synthesizer output files into Industry standard Sign off Timing/Power Analysis tools		
9	Cross-probing between HDL, schematic and Industry standard timing & power reports/database with GUI support		
10	Support for Pipeline and general register retiming		
11	Support for Designware/Chipware/Similar <Vendor>ware functional components and simulation models		
12	Support for entire design DFT logic insertion and optimization		
13	Support for Concurrent Multimode Multi Corner timing analysis and optimization		
14	Support for Advanced datapath/Arithmetic optimization techniques for better QoR based on the required user application		
15	Ability to re-synthesize, restructure and optimize the critical path on an incremental basis at various stages of RTL to Gate level conversion		
16	Ability to support automatic mapping of the complex library elements present in the technology library for better QoR along with extensive flexibility for users to control the complex cell insertion and QoR analysis		
17	Support for multi-threading on multi-core processors/distributed processing over network/ CPU acceleration for faster synthesis turnaroundtime (Default base license should support at least 8 CPU cores and option to increase more with additional CPU acceleration licenses)		
Sub Category-C2: Physically Aware Synthesis			
1	Physically aware logic structure and mapping with results correlation within 5 -10% of physical		

	implementation		
2	Should perform global synthesis optimization using real physical wire delay		
3	Should eliminate the need to add excessive timing margin during synthesis, enabling further power and area reduction		
4	Should present physical feedback to logic designer to help drive corrective action during synthesis		
5	Should support Native congestion modeling to enable automatic congestion optimization, analysis and fixing.		
6	Morphing and Demorphing for congestion optimization		
7	Congestion aware DFT logic placement		
8	Should support Top down register retiming balance logic across the registers, maximizing the data throughput in single-pass synthesis run		
9	Should support Physical aware clock gating		
10	Should support Physical aware logic structuring on congested SOC, improves total negative slack , area , wire length & power		
11	Should support Physical aware mapping to improve worst negative slack, total negative slack and congestion		
12	Physical Multibit inferencing to improve the leakage power		
13	Should support Physical aware Engineering Change Order (ECO)		
14	Should support Physical aware DFT synthesis		
Sub Category-C3: Low Power Synthesis			
1	IEEE 1801 based low power design flow		
2	Multi-Vt insertion/optimization based on design constraints and optimization directives		
3	Hierarchical RTL Clock gating, operand isolation, DVFS, Power Shut-off etc		
4	Automatic power domain aware insertion of level shifters, isolation cells, retention elements and Header/Footer switches		
5	Always on buffering and power domain aware routing		

19.5 Specifications compliance form: Floorplanning, Partitioning, Place & Route Solution

Sl. No.	Specifications	Compliance (Yes/No)	Remarks
Sub Category-D1: Floorplanning, Place and Route			
1	Support for Hierarchical/Flat HDL designs of gate sizes ≥ 75Million gate instances, exclusive of hard macros		
2	Support for ❖ Silicon virtual prototyping ❖ Interactive & Automatic design Floorplanning ❖ Physical synthesis ❖ Design partitioning, pin assignment & timing budgeting ❖ Legal macro & standard cell placement ❖ Power grid design & optimization ❖ Hierarchical CTS ❖ Feed-through insertion, pipeline registers, clock planning		
3	Support for automatic floor plan generation for optimal timing, power, area and congestion results with floor plan ranking capabilities		
4	Support for Congestion, Timing and power-driven logic re-synthesis & placement		
5	Support for tight timing correlation between Synthesis and placement		
6	Support for concurrent clock and data optimization		
7	Support for bottom-up, top-down hierarchical methodologies with black box modeling support		
8	Support for concurrent macro and standard cell placement		
9	GUI support for timing, power and clock debug & diagnostics		
10	Support for Clock Mesh capabilities for clock tree synthesis to achieve low skew and high OCV tolerance		
11	Support for slack driven placement		
12	Support for flip-chip RDL routing capabilities		
13	Support for concurrent physical and electrical optimization of clock and data paths in the design		
14	Support for automatic congestion resolving capabilities and pin access by intelligent		

	placement/spacing of standard cells		
15	Support for vector/vectorless based dynamic and leakage power optimization		
16	Support for optimal routing convergence on timing, area, power, signal integrity and manufacturing goals		
17	Support for concurrent Via pillar optimization and enhancement		
18	Support for tight correlation between pre-route and post route analysis		
19	Support for Multi Mode Multi Corner analysis of the design		
20	Support for Multi Corner Clock Tree synthesis		
21	Support for ECO at RTL and Netlist level		
22	Support to map/place/route ECO cells without affecting QoR		
23	Support for Master clone in place optimization		
24	Support for IR drop aware placement and power integrity in the flow		
25	Support for parallel bus routing, 3D shielding, length matching, differential pair routing and resistance matching		
26	Support for all industry standard input and output formats for following		
27	GUI support for the entire place and route flow from netlist to GDSII		
28	Support for machine learning for better QoR		
29	Distributed multi-CPU and multithreaded processing for maximum hardware utilization (Default base license should support at least 8 CPU cores and option to increase more with additional CPU acceleration licenses)		
Sub Category-D2: Low Power Support			
1	IEEE 1801 support		
2	End-to-end multi-supply voltage (MSV) support		
3	Power domain-aware automatic floor plan synthesis		
4	Power domain-aware routing		
5	Dynamic Voltage Frequency Scaling support (DVFS)		
6	Power shut-off and power switch prototyping		

7	State Retention Power Gating support		
8	Always-on buffer support		
9	Hierarchical Macro Model support		
Sub Category-D3 : Advance node features			
1	32/28/20/16/14nm support in routing and verify		
2	Fully certified down to 14nm at leading foundries		
3	FinFet Support - Support for color aware routing for timing improvement in lower technology nodes		
4	DPT conflict and DRC check features		
5	Context-driven placement &Structured datapath support considering advanced node placement & routing requirements		
6	DFM/DFY optimization for wires, cell, vias		
7	Critical area for yield analysis		
8	Litho-aware routing with prevention and fixing		
9	1-D routing support		
10	Clock mesh & hybrid implementation		

19.6 Specifications compliance form: Signoff Timing Solution

Sl. No.	Specifications	Compliance (Yes/No)	Remarks
1	Fully certified down to 14nm at leading foundries		
2	Concurrent multi-mode and multi corner support		
3	Integration with Power Sign off engine for running IR aware STA		
4	Support for placement aware timing analysis - timing analysis considering location and length of a path being analyzed		
5	Support signoff-accurate and physically aware timing ECO		
6	Support for integrated parasitic extraction and power analysis functionality		
7	Support for interactive cross-probing functionality		
8	Support for overlap and crosstalk effects to ensure proper signal integrity		
9	Support for OCV & AOCV to reduce unwarranted pessimism caused by on-chip variation		
10	Support for statistical static timing analysis by considering logic correlation between signals		

11	Analyze a part of a design independent of the whole design without losing QOR		
12	Ability to analyze and report false violations		
13	Availability of reference flow or example designs (14nm node preferred)		
14	Global timing debug to accelerate root-cause and bottleneck analysis		
15	Physically aware engineering change order (ECO) optimization for MMMC		
16	MMMC-aware timing debug for quick timing issue identification across all views		
17	MMMC signoff ECO optimization and repair across all timing views for fewer ECO cycles. The Physical Aware capability of the tool should allow a signoff timing closure in about 2-3 ECO cycles		
18	Distributed multi-CPU and multithreaded processing for maximum hardware utilization (Default base license should support at least 8 CPU cores and option to extend on additional CPU's with additional CPU acceleration licensing)		

19.7 Specifications compliance form: Signoff Power Solution

Sl. No.	Specifications	Compliance (Yes/No)	Remarks
1	Fully certified down to 14nm at leading foundries		
2	Calculation and analysis of power consumption, including leakage, internal, and switching power		
3	Calculation of vector/vector-less leakage and dynamic power analysis		
4	Calculate peak and average power		
5	Analyze the design for low power		
6	Analysis of the full-chip resistance network, including effective and least resistance		
7	Create physical-aware power-density vector profiles		
8	Analyze and optimize EM and IR drop effects		
9	Carry out hybrid, mixed-mode analysis in the combination of gate/RTL vectors and vector-less		
10	Vector-based analysis, including gate/RTL-level VCD/FSDB, test scan-mode, etc.		
11	Perform De-coupling cap analysis and optimization		

12	Analysis of the impact of power on design closure, from chip to package and PCB		
13	Should support industry-standard NLDM and CCS Power libraries		
14	Supports voltage and temperature scaling to create unique PVT points from a restricted library		
15	Simultaneous and complete analysis of all cross-domain paths under all scenarios		
16	Calculate block level power analysis		
17	Static Early Rail Analysis using power grid views		
18	Support for Chip-package models		
19	What-If analysis for static power & power rail R		
20	Tight integration with Digital implementation and STA engine		
21	Interactive reports & plots		
22	Dynamic IR drop and EM analysis		
23	Vector-driven & vector less dynamic power & power distribution calculation		
24	Dynamic Early Rail Analysis using power grid views		
25	Analysis of de-coupling capacitance & rush-current		
26	What-If analysis dynamic power, power rail RC, de-coupling capacitance		
27	Integration with STA engine for running IR aware STA		
28	Missing via checks on Power Network Optimization		
29	Clock tree power estimation		
30	Distributed multi-CPU and multithreaded processing for maximum hardware utilization (Default base license should support at least 16 CPU cores without additional licensing)		

19.8 Specifications compliance form: DFT & ATPG Solution

Sl. No.	Specifications	Compliance (Yes/No)	Remarks
Sub Category-G1 : DFT			
1	Foundry support down to 14nm		
2	Support for full and partial scan insertion		
3	Support for timing aware test point insertion		

4	Support for physically aware scan-chain stitching		
5	Support for power aware timing pattern generation		
6	Provide automatic timing constraints for DFT-related paths for faster timing closure		
7	Should have Advanced DFT rule checking, Tristate rules , shift register rules , clock rule , async reset/set violation, abstract segment violation		
8	IEEE1500 core wrapping methodology for big SOCs		
9	Boundary scans (IEEE1149.1 & IEEE1149.6) insertion for digital and analog IOs		
10	Test Point analysis and optimization (RRFA/DFA) deterministic fault analysis and random resistance fault analysis for better ATPG patterns and coverage		
11	Support for test compression features to reduce test time and pattern volume without reducing fault coverage figures		
12	Should support Smart Scan multi-site test, Low power Multi-segment scan. Smart scan is low pin count testing which helps to test multiple devices		
13	Smart scan compression with serializer/de-serializer logic in built to achieve low pin count compression		
14	Low Pin count test		
15	Support for at speed testing using on-chip PLL		
16	Power aware test access mechanism with IEEE 1801 to enable the testing of the low power structures in design and generation of the ATPG based on power modes in design		
17	Should have single pass fully integrated DFT flow in synthesis		
Sub Category-G2 : ATPG			
1	Should support Static test for Full scan, partial scan and sequential ATPG for edge-triggered and LSSD design		
2	Integrated test pattern generation for Static, IDDQ, and I/O parametric fault models		
3	Support for Timed (SDC and SDF) delay, small		

	delay, and physically aware bridge fault models		
4	Should support Core-based testing, test data migration and test reuse		
5	Special support for custom designs such as data pipelines, scan control pipelines, and scan safe to insert lock-up latches for a skew safe scan design		
6	Net bridging feature - Potential bridge candidate based on net adjacency to be modeled as bridging faults		
7	Should support ATPG with power targets during scan and capture events of ATPG		
8	Support pattern generation for RAM sequential test		
9	Low-power ATPG with scan and capture toggle count limits		
10	Distributed CPU support for parallel processing of ATPG		
11	Support for user defined fault model at primitive cell, hierarchical block or cell instance levels		
12	GUI with interactive analysis capabilities like scan chain tracing and the test coverage analysis		
Sub Category-G3 : MBIST			
1	Unified Programmable MBIST engine with programmable capabilities; User programmable algorithms test time applied and modified through the TAP		
2	Flexibility for PMBIST logic sharing		
3	Verilog testbench generation for validation in a Verilog simulator		
4	Support for embedded SRAMs, ROMs, Register Files, unrestricted multiple ports		
5	Flexible MBIST interface: Direct Access and JTAG		
6	Rich predefined hardcoded memory test algorithms		
7	Supports Diagnostics, redundancy repair analysis		
8	Support for Soft Repair and interface to hard repair solutions using soft repair interface		
9	Support top bottom and bottom up MBIST design insertion flows		
10	Flexible scheduling (test plan) of MBIST engines		
Sub Category-G4 : LBIST			
1	LBIST with test point insertion for coverage for		

	automotive and defense devices		
2	Direct access Logic BIST, JTAG controlled Logic BIST with hierarchical LBIST solution		
3	Clock staggering in LBIST mode for reducing the power during LBIST scan mode		
4	Lowest area overhead		
5	LBIST running at input oscillator frequency		
6	Ability to test the LBIST Macro; support for asynchronous set and reset clock testing.		
7	Full automated solution with logic synthesis		
8	Netlist insertion, connectivity, verification and signature generation		

19.9 Specifications compliance form: Extraction & Physical Verification Solution

Sl. No.	Specifications	Compliance (Yes/No)	Remarks
Sub Category-H1 : RC Extraction			
1	Support for Black-box, gray-box, or white-box extraction modes		
2	Lumped R only, C only, or RC for all nets		
3	Coupled C for all nets		
4	Self (L) and mutual (K) inductance extraction		
5	Fully-distributed RC and RLCK for all nets		
6	RLCK for selected nets and C for the rest, or vice versa		
7	Hierarchical transistor-level RC extraction		
8	Ability to exclude nets, such as power and ground nets		
9	Critical net and critical path extraction		
10	Supports both transistor-level and cell-level extractions during design implementation and signoff.		
11	Integrates seamlessly with both Analog custom design and digital implementation platforms for better productivity enhancement		
12	Unlimited Transistor support- There should be no limitation of licensing for design size		
13	Unlimited Cell Instances Support-There should be no limitation of licensing for design size		
14	Hierarchical Transistor support - There should be no limitation of licensing for design		

	hierarchy. Same license supports flat & hierarchical design extraction		
15	Wire Edge Enlargement support		
16	Separate bias for Capacitance and Resistance		
17	Virtual Metal Fill option		
18	Temperature dependent Resistance extraction option		
19	Thickness (density) support- For lower node designs (65 & below) dielectric and metal thickness effects to be considered in extraction		
20	Multiple Process Corners support		
21	Thickness f(d, w) support- For lower node designs (65 & below) dielectric and metal thickness effects to be considered in extraction		
22	Field Solver (transistor & cell) support for most accurate capacitance extraction		
23	Inductance extraction at cell level		
24	Substrate Extraction (RC extraction)		
25	Via Effect Extraction		
26	Loading Effect Extraction		
27	Contact Bias 2D Table (Po-Co spacing, Co-Co spacing)		
28	Advanced Modeling features (40nm to 14nm)		
29	Multiple retargeting tables support (28, 22nm)		
30	Coplanar Metal capacitance support		
31	Via Temp dependent temperature coefficient f(area)		
32	Slot Vis support		
33	Flexible Cap & Res modeling		
34	OPC-WEE support		
35	2-bias contact support and Contact Dual Bias support		
36	All advanced node modelling effects support for FinFet technologies up to 16FF to be supported		
37	Certified at all leading foundries for all the nodes up to 16FF		
38	Distributed Processing support		
39	Multi CPU support for acceleration		
Sub Category-H2 : DRC Verification			
1	Should be foundry qualified and certified DRC solution at leading foundries across the process		

	technologies, specially at advanced nodes from 28nm to 14nm		
2	Should enable DRC, Antenna, XOR, Fast XOR and Fill capabilities- Fast XOR is for GDS vs. GDS compare		
3	Signoff DRC check based on foundry rules		
4	Support complex rules checking		
5	Integration within Analog Layout, Digital Implementation environments		
6	Ability to read/write presets for different form values in GUI- Auto form filling with default values		
7	Support limited area checks, by coordinates		
8	Support configuration of custom rules		
9	Support DRC checks on GDS, Open Access, OASIS formats		
10	GUI and command line support		
11	Support distributed processing and multi-threading		
12	Support DRC on Original Layers, Derived Layers		
13	Support grouping of rules by rules		
14	Support conditional checks		
15	Support select/unselect checks by DRC rules		
16	Support reporting of results in different formats i.e. GDS, ASCII, OASIS, OA format		
17	Support flat/hierarchical DRC run		
18	Support 32/64 bit processing		
19	Option to provide maximum number of errors in report		
20	Highlight errors in different colors		
21	Should allow debugging of results while DRC is running - As DRC is still running, the completed DRC results should be viewed and start fixing the layout.		
22	Ability to exclude cells during DRC run		
23	Ability to show flat/hierarchical counts of DRC errors		
24	Support for LELE/SADP, DPT, TPT, QPT		
25	Support for Loop detect, 3D IC, advanced Metal Fill,		
26	Support for DFM fill, Track based Fill,		

27	Support for Voltage Dependent Rules, FinFet		
Sub Category-H3 : LVS Verification			
1	Should be foundry qualified and certified LVS solution at leading foundries across the process technologies, specially at advanced nodes from 28nm to 14nm		
2	Enable Layout vs Schematic checks		
3	Compare GDSII to Netlist, Netlist to netlist		
4	Support 32/64 bit processing		
5	Support distributed processing		
6	Integration within Analog, Digital design environments		
7	GUI and command line support		
8	Support GDSII, OASIS, DFII as layout source		
9	Support CDL/Spice/Verilog inputs as schematic source		
10	Support for power/ground connections on leaf cells		
11	Flat and hierarchical run capabilities		
12	Support extraction of layout Netlist from GDSII, Layout		
13	Ability to create ASCII database for connectivity extraction		
14	Support creation of single netlist from different input formats (CDL/Spice/Verilog)		
15	Option to provide maximum number of errors in report		
16	Ability to create summary/report in detailed format- format for summary/report is Text (All reports) , ASCII, GDS, OASIS (ERC – Electrical rule check reports)		
17	Support identification for Soft Check errors		
18	Support virtual connect rules for unconnected nets		
19	Support identification of opens/Shorts		
20	Support identification of Power/Ground shorts		
21	Support reporting of Malformed devices		
22	Support recognition of gates i.e. simple and all		
23	Support auto match capability for automatic matching- matching of cell names in layout & schematic		

24	Support hcells to be defined during LVS for name mismatch in source and layout		
25	Support automatic generation of hcells		
26	Support definitions of Power/Ground net names for extraction		
27	Ability to ignore port names during comparison		
28	Support filtering of devices from netlist based on device connectivity		
29	Support definition of black box cells		
30	Support for Stamping Conflict Debug		
31	Graphical LVS debus support		
32	FinFET parameter genFIN, LDE support		
33	Device signature support		
34	3D IC (LVS related) support		
35	Advanced device parameter support		

19.10 Terms compliance: Installation, Training and Licensing

Sl. No.	Specifications	Compliance (Yes/No)	Remarks
1	Installation and provide complete training, tutorials at C-DAC, Thiruvananthapuram		
2	Full flow has to be provided by the single bidder for better integration and application support across the project		
3	Vendor has to provide additional trainings and tool related flow support during the AMC period as requested by C-DAC		
4	Vendor should be able to accommodate any change in license quantities (between purchased products not exceeding the overall cost)		
5	Vendor has to submit relevant foundry signoff certifications and customer success references flow using the tool chains quoted at advanced node up to 14nm		
6	Training and tutorials should cover all design, functional, feature aspects of the offered solution and should be provided directly by the application engineers from OEM		
7	The offered solution must be tested for all the specifications prior to installation/ delivery		
8	Operating System: Linux/Unix		

9	**Licensing Scheme for Category-A: Verification Solution**			
	Sub Category -A1: Logic Simulation Tool			
	1	240 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	8 countrywide floating perpetual licenses inclusive of 1 year AMC		
	Sub Category -A2: Low power support			
	1	12 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	1 countrywide floating perpetual licenses inclusive of 1 year AMC		
	Sub Category -A3: Formal Verification			
	1	1 countrywide floating perpetual licenses inclusive of 1 year AMC		
10	**Licensing Scheme for Category-B:Logic Equivalence Checking Solution**			
	Sub Category -B1: Logic Equivalence Checks			
	1	72 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC		
	Sub Category-B2: Low Power Logic Equivalence Checks			
	1	12 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	1 countrywide floating perpetual licenses inclusive of 1 year AMC		
	Sub Category-B3: Logic Equivalence Check ECO flow			
	1	12 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	1 countrywide floating perpetual licenses inclusive of 1 year AMC		

11	**Licensing Scheme for Category-C: RTL Synthesis Solution**			
	Sub Category -C1: RTL Synthesis			
	1	48 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	3 countrywide floating perpetual licenses inclusive of 1 year AMC		
	Sub Category-C2: Physically Aware Synthesis			
	1	48 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	3 countrywide floating perpetual licenses inclusive of 1 year AMC		
	Sub Category-C3: Low Power Synthesis			
	1	12 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	1 countrywide floating perpetual licenses inclusive of 1 year AMC		
12	**Licensing Scheme for Category-D:Floorplanning, Partitioning Place & Route Solution:**			
	Sub Category-D1: Floorplanning, Place and Route			
	1	84 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	4 countrywide floating perpetual licenses inclusive of 1 year AMC		
	Sub Category-D2: Low Power Support			
	1	12 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	1 countrywide floating perpetual licenses inclusive of 1 year AMC		
	Sub Category-D3 : Advance node features			
	1	42 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of		

		each license		
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC		
13	**Licensing Scheme for Category-E: Signoff Timing Solution:**			
	1	84 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	4 countrywide floating perpetual licenses inclusive of 1 year AMC		
14	**Licensing Scheme for Category-F: Signoff Power Solution:**			
	1	42 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC		
15	**Licensing Scheme for Category-G: DFT & ATPG Solution:**			
	Sub Category-G1 : DFT			
	1	12 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC		
	Sub Category-G2 : ATPG			
	1	12 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC		
	Sub Category-G3 : MBIST			
	1	6 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	1 countrywide floating perpetual licenses inclusive of 1 year AMC		
	Sub Category-G4 : LBIST			

	1	6 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	1 countrywide floating perpetual licenses inclusive of 1 year AMC		
16	**Licensing Scheme for Category-H: Extraction & Physical Verification Solution:**			
	Sub Category-H1 : RC Extraction			
	1	72 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC		
	Sub Category-H2 : DRC Verification			
	1	72 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC		
	Sub Category-H3 : LVS Verification			
	1	72 countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license		
	2	2 countrywide floating perpetual licenses inclusive of 1 year AMC		

19.11 Terms compliance: Customer Support

Sl. No.	Specifications	Compliance (Yes/No)	Remarks
1	Support should be provided by the respective OEMs of each items directly. C-DAC should be able to raise the support queries with the OEM Field application engineers directly through email or online support portals.		
2	Full technical support with complete documentation/white papers and video tutorials. Support should be provided through Email/Fax/support system and depending on the gravity of the problem, Field Application		

	engineer shall visit C-DAC for solution of problem on mutually agreeable basis.		
3	OEM shall carry out any number of emergency visits during warranty and AMC period as and when required. The maximum response time from OEM must not be more than 48 hours (excluding holiday).		
4	All expenses on the visit(s) of the OEM's engineer such as to and fro travel costs, local transportation, boarding and lodging etc. during warranty and AMC period shall be borne by the OEM/Contractor.		
5	OEM should regularly provide & install upgrades, updates, service packs, patches of the Software Products, released during the warranty period, even if the existing capabilities of the licensed software are enhanced / released with a different brand name/trade mark.		
6	C-DAC should be provided with the online on-demand tutorials, study materials, documents, databases, advanced online learning courses available as part of the training material for the entire solution offered against each of the specification during the entire AMC period		
7	Since the purchase is primarily intended for a mission critical project, in addition to the regular support services provided by the OEM, a one point contact window should be assigned for C-DAC for the entire AMC period by OEM who is well versed in RTL to GDSII design & tape out technology nodes up to 14nm.		

19.12 Pro forma of Bank Guarantee for EMD

Whereas _____ (hereinafter called "the Bidder") has submitted its bids dated _____ for "The Tender (CDACT.PHS.RD.HDG083D.279.19-20) for _____" at Centre for Development of Advanced Computing (hereinafter called "the Bid").

KNOW ALL MEN by these presents that WE _____ of_____ _____ having our registered office at_____ _____ (hereinafter called "the Bank") are bound unto the Section Head (Purchase), Centre for Development of Advanced Computing, P B No 6520, Vellayambalam, Thiruvananthapuram - 695033, Kerala (hereinafter called "C-DAC") in the sum of _____ for which payment well and truly to be made to the said C-DAC, the Bank binds itself, its successors and assigns by these presents.

THE CONDITIONS of this obligation are:

1. If the Bidder, having its bid during the period of bid validity specified by the Bidder on the Bid Form; or
2. If the Bidder, having been notified of the acceptance of its Bid by C-DAC during the period of bid validity
   a) Fails or refuses to accept the Letter of Award of the project within the specified time
   b) Fails or refuses to furnish the Performance Security within the specified time
   c) Fails or refuses to execute Contract Agreement

We undertake to pay to C-DAC up to the above amount upon receipt of its first written demand, without C-DAC having to substantiate its demand, provided that in its demand C-DAC will note that the amount claimed by it is due to it owing to the occurrence of one or both of the two conditions, specifying the occurred condition or conditions.

This guarantee will remain in force up to and including 45 days after the period of bid validity and any demand in respect thereof should reach the Bank not later than the above date.

Sealed with common seal of the said Bank this _____ day of _____ 2019

_____

(Authorized Signatory of the Bank)

19.13 Pro forma of Bid Securing Declaration

< In Bidders letter head >

Date: [Insert: date of bid]
e-Tender No: CDACT.PHS.RD.HDG 083D.279.19-20

From
(Registered name and address of the bidder)
To:
THE HEAD, PURCHASE SECTION
CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING
VELLAYAMBALAM
THIRUVANANTHAPURAM – 695033

Bid securing undertaking declaration

We, the undersigned on behalf of and under the authority of M/s ……(herein after referred to as bidder) hereby undertakes to declare:

1. That we, the bidder understand that, vide clause 5.26 in section 5 of the RFP cited above , bids can be supported with a Bid Securing Declaration, in lieu of submitting Earnest Money Deposit specified in the said clause as attached at section 9.12 of the said RFP and
2. That we, the bidder understand that, we shall be automatically be suspended from being eligible for bidding in any contract with the Centre for Development of Advanced Computing(C-DAC) (herein after referred to as Purchaser) for a period of 3 years/or for a period as decided by the competent authority, commencing from the closing date of bid submission, on breach, by the bidder, of any of the following obligation(s) under the bid conditions:-
   i. On withdrawal from the proposal or on enhancement of the quoted price subsequent to the bid opening and/or during the Bid validity period or of its extended period, if any.
   ii. On failing to accept and/or execute the contract after being the successful bidder in accordance with the terms and conditions (including timelines for execution of the Agreement) of the said RFP/Purchase Order issued thereof or on failure to furnish the performance security in accordance with the terms and conditions (including timelines for furnishing performance security) of the said RFP/purchase order issued thereof.
   iii. On indulging in any act that would jeopardize or unnecessarily delay the process of bid evaluation/finalization/execution of the proposed contract in accordance with timelines as specified by the purchaser.
3. That we, the Bidder understand that this declaration shall expire on our not being a successful Bidder and on notice of the award of the said contract to another Bidder or thirty days after the validity of the Bid; whichever matures earlier.

(Signature)
Authorized Signatory
Name :
Designation :
Office Seal :
Place :
Date :

20 Price Bid

Commercial Bid shall be submitted online as described in Annexure-B.

1 Commercial Bid covering letter
2 Price bid as per BoQ.xls duly filled

1. Commercial Bid Covering Letter Template

< In Bidders letter head >

Date: [Insert: date of bid]
From
(Registered name and address of the bidder)
To:
THE HEAD, PURCHASE SECTION
CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING
VELLAYAMBALAM
THIRUVANANTHAPURAM – 695033

Dear Sir,
Having examined Tender Document number CDACT.PHS.RD.HDG083D.279.19-20 dated _____ the receipt of which is hereby acknowledged, we, the undersigned, offer supply, installation & commissioning and operationalisation of …….. (meaning as realized in Tender Document) at C-DAC, in full conformity with the said Tender Document, for a total project cost of …… (…….. only). The above amount is in accordance with the Price Schedules herewith made part of this bid as per the price bid template.

1. We undertake that we shall successfully setup and demonstrate the solution offered to C-DAC in conformity with the bidding documents (and as amended from time to time) for a total cost as provided in the price bid if the contract is awarded to us.

2. We declare that we have studied Tender Document and are making this proposal with a stipulation that you shall award us Contracts, either in part or whole, for the supply, installation, implementation, Integration & commissioning and operationalisation of **EDA TOOLS FOR DIGITAL IC DESIGN & TAPE-OUT (EDA-ICD)** in deep submicron technology nodes for complex digital system designs at C-DAC, identifying separately including all other services specified in the Contract Documents.

3. We have read the provisions of Tender Document and confirm that these are acceptable to us. All necessary clarifications, if any, have been sought for by us and duly clarified in

writing, by C-DAC, Thiruvananthapuram. We understand that any other ambiguous clauses in the Tender Document, if any, are subject to interpretation of C-DAC (T).

4. We undertake, if our bid is accepted, to commence the work on the project immediately upon your Notification of Award to us, and to achieve Completion within the time stated in the Bidding Documents.

5. If our bid is accepted, we undertake to execute all contractual documents and provide all securities & guarantees as required in the bid document (and as amended from time to time).

6. We undertake that, in competing for (and, if the award is made to us, in executing) the above contract, we will strictly observe the laws against fraud and corruption in force in India namely "Prevention of Corruption Act".

7. We agree to abide by this bid, consisting of this letter, the tender fee, Bid Securing Declaration, EMD, Technical bid, for a period of bid validity from the date fixed for submission of bids as stipulated in the Tender Document, and it shall remain binding upon us and may be accepted by you at any time before the expiration of that period.

Dated this [insert: number] day of [insert: month], [insert: year] Signed: …….
In the Capacity of [insert: title of position]

Duly authorized to sign this bid for and on behalf of [insert: name of the Bidder]

Witness:
Address:

Annexure-A: MAC and QCC form

A.1 Minimum Acceptance Criteria (MAC) Compliance Form

Sl. No	Requirements	Document Code	Documents Submitted (Y/N)
1	Operation for a period of at least 3 years in India a. Certificate of Incorporation.	D01	
	b. Annual Reports for the last 3 years.	D02	
2	A Certificate from the OEM Company Board on a Company's letter head with a reference number and date certifying that the Bid signatory is authorized by the Company.	D03	
3	A Certificate from the OEM Company, on a OEM Company's letter head having reference number and date, certifying that the agent is authorized to Bid on their behalf and the signatory is authorized by the Company to do so.	D04	
4	Certificate from the Company authorized signatory to the effect that the bidder and the OEM company are not blacklisted by any of the Ministry/Department of Government of India/ State Governments.	D05	
5	EMD as Unique Transaction Reference Number/DD or BG bank certificate/Bid Securing Declaration/MSME or NSIC certificate submitted	D06	
6	a. Copy of PAN	D07	
	b. Copy of TAN	D08	
	c. Copy of GST document	D09	
7	Bid validity Declaration for 120 days	D10	

A.2 Qualification Clause Compliance (QCC) form

Sl. No	Qualification Clauses	Compliance (Y/N)
1	Agree to supply evaluation licenses of the tools for the finalization of the proposed solution.	
2	Agree to provide flexibility on the start date of the licenses during the project tenure.	
3	Agree to offer a solution which would work as a standalone tool without any dependency on the tools of other categories.	
4	Comply that C-DAC reserves the rights to withdraw the Tender at any time without assigning any reason.	
5	Quote should comply with all the mandatory specifications.	
6	Provide the performance data of the completed designs along with self-certification or satisfactory completion certificate from the customers who have completed designs using the offered solution for a design size of not less than 75million gates instances.	
7	Provide the necessary documents, video tutorials, access to on-demand tutorials, databases, advanced online learning courses of the solution offered.	
8	Agree to install, setup and demonstrate the entire features of the offered solution with sample database	
9	Agree to provide the necessary training on the offered solution and its management to C-DAC team	
10	Agree to provide the technical support to C-DAC team members for the license period after the installation of licenses in C-DAC	
11	Agree to supply all updates to the offered Tools during the AMC/Warranty period without any additional cost.	
12	Provide C-DAC the rights to procure each category of tools independently	
13	Comply with the LD clauses	
14	Minimum number of orders of same/similar(containing predominant nature of tendered work) type executed (not less than Three executed orders of not less than amount equal to Rs.4 crores/Two executed orders of not less than Rs.5crores/One executed order of not less than Rs.8 crores).Valid and relevant documentary evidence to be submitted.	
15	Quality Accreditation/ Approved license	

Signature
(Company's authorized person)
Name:
Designation:

(Company's seal)

Annexure-B: Instructions for Online Submission

The bidders are required to submit soft copies of their bids electronically on the CPP Portal, using valid Digital Signature Certificates. The instructions given below are meant to assist the bidders in registering on the CPP Portal, prepare their bids in accordance with the requirements and submitting their bids online on the CPP Portal. More information useful for submitting online bids on the CPP Portal may be obtained at: https://eprocure.gov.in/eprocure/app.

B.1 Registration:

a. Bidders are required to enroll on the e-Procurement module of the Central Public Procurement Portal (url: https://eprocure.gov.in/eprocure/app) by clicking on the link `Click here to Enroll'. Enrolment on the CPP Portal is free of charge.
b. As part of the enrolment process, the bidders will be required to choose a unique username and assign a password for their accounts.
c. Bidders are advised to register their valid email address and mobile numbers as part of the registration process. These would be used for any communication from the CPP Portal.
d. Upon enrolment, the bidders will be required to register their valid Digital Signature Certificate (Class II or Class III Certificates with signing key usage) issued by any Certifying Authority recognized by CCA India with their profile.
e. Only one valid DSC should be registered by a bidder. Please note that the bidders are responsible to ensure that they do not lend their DSCs to others, which may lead to misuse.
f. Bidder then logs into the site through the secured login by entering their user ID/ password and the password of the DSC / eToken.

B.2 Searching for tender documents:

a. There are various search options built in the CPP Portal, to facilitate bidders to search active tenders by several parameters. These parameters could include Tender ID, organization name, location, date, value, etc. There is also an option of advanced search for tenders, wherein the bidders may combine a number of search parameters such as organization name, form of contract, location, date, other keywords etc. to search for a tender published on the CPP Portal.
b. Once the bidders have selected the tenders they are interested in, they may download the required documents / tender schedules. These tenders can be moved to the respective `My Tenders' folder. This would enable the CPP Portal to intimate the bidders through SMS / E-mail in case there is any corrigendum issued to the tender document.

c. The bidder should make a note of the unique Tender ID assigned to each tender, in case they want to obtain any clarification / help from the Helpdesk.

B.3 Preparation of bids:

a. Bidder should take into account any corrigendum published on the tender document before submitting their bids.
b. Please go through the tender advertisement and the tender document carefully to understand the documents required to be submitted as part of the bid. Please note carefully, the number of covers in which the bid documents have to be submitted, the number of documents – including the names and content of each of the document that need to be submitted. Any deviations from these may lead to rejection of the bid.
c. Bidder, in advance, should get ready the bid documents to be submitted as indicated in the tender document /schedule and generally, they can be in PDF / XLS / RAR / DWF formats. Bid documents may be scanned with 100dpi with black and white option.
d. To avoid the time and effort required in uploading the same set of standard documents which are required to be submitted as a part of every bid, a provision of uploading such standard documents (e.g. PAN card copy, annual reports, auditor certificates etc.) Has been provided to the bidders. Bidders can use `My Space' area available to them to upload such documents. These documents may be directly submitted from the `My Space' area while submitting a bid, and need not be uploaded again and again. This will lead to a reduction in the time required for bid submission process.

B.4 Submission of bids:

a. Bidder should log into the site well in advance for bid submission so that he/she is able to upload the bid in time i.e. on or before the bid submission time. Bidder will be responsible for any delay.
b. The bidder has to digitally sign and upload the required bid documents one by one as indicated in the tender document.
c. Bidder has to select the payment option as `offline' to pay the tender fee / EMD as applicable and enter details of the instrument(s). Bidder can pay Tender Fee/EMD through NEFT and submit the Unique Transaction Reference Number instead.
d. The system time (which is displayed on the bidders' dashboard) will be considered as the standard time for referencing the deadlines for submission of the bids by the bidders, opening of bids etc. The bidders should follow this time during bid submission,
e. All the documents being submitted by the bidders would be encrypted using PKI encryption techniques to ensure the secrecy of the data. The data entered cannot be viewed by unauthorized persons until the time of bid opening. The confidentiality of the bids is maintained using the secured Socket Layer 128 bit encryption technology. Data storage encryption of sensitive fields is done.

f. The uploaded tender documents become readable only after the tender opening by the authorized bid openers.

g. Upon the successful and timely submission of bids, the portal will give a successful bid submission message and a bid summary will be displayed with the bid no. and the date & time of submission of the bid with all other relevant details.

B.5 Assistance to bidders:

a. Any queries relating to the tender document and the terms and conditions contained therein should be addressed to the Tender Inviting Authority for a tender or the relevant contact person indicated in the Tender.

b. Any queries relating to the process of online bid submission or queries relating to CPP Portal in general may be directed to the 24*7 CPP Portal Helpdesk. The contact number for the helpdesk is 1800 233 7315.

B.6 General instructions to the bidders:

a. The bids will be received online through portal https://eprocure.gov.in/eprocure/app. In **the Technical Bids, the bidders are required to upload all the documents in .pdf format.**

b. Possession of Valid Class II/III Digital Signature Certificate (DSC) in the form of smart Card /e-Token in the company's name is a prerequisite for registration and participating in the bid submission activities through https://eprocure.gov.in/eprocure/app. Digital Signature Certificates can be obtained from the authorized certifying agencies, details of which are available in the web site https://eprocure.gov.in/eprocure/app under the link `Information about DSC'.

c. Bidders are advised to follow the instructions provided in the `Instructions to the Bidders for the e-Submission of the bids online through the Central Public Procurement Portal for e-Procurement at https://eprocure.gov.in/eprocure/app.

Annexure-C: Technical Evaluation Procedure & Compliance form

C.1 Technical Evaluation Procedure

As part of the tool evaluation process the vendor should demonstrate all the specifications mentioned under the respective category for which the vendor has placed the bid on a standard design integrating logic instances and hard macros.

C.2 Technical Evaluation Compliance Form

Sl. no	Category	Compliance (Y/N/NA)
1	Verification Solution	
2	Logic Equivalence Checking Solution	
3	RTL Synthesis Solution	
4	Floorplanning, Partitioning, Place & Route Solution	
5	Signoff Timing Solution	
6	Signoff Power Solution	
7	DFT&ATPG solution	
8	Extraction & Physical Verification Solution	

Annexure-D: Checklist

Sl. No.	Documents	Y/N
1	Scanned copy of the Demand draft towards tender fee or Exemption Certificate for Tender fee	
2	Scanned copy of Bid Securing Declaration/Unique Transaction Reference Number/Demand Draft/BG/Exemption Certificate towards Earnest Money Deposit along with EMD details (refer 19.1)	
3	Pre-qualification criteria supporting documents (refer Section 19)	
4	Technical Compliance and Support documents (refer Section 19)	
5	Financial and Undertaking documents (refer Section 19)	
6	Commercial Bid Covering Letter (refer Section 20)	
7	BoQ.xls	

Annexure-E: Financial Information

Particulars	Financial Year		
	2016-17	2017-18	2018-19
Annual Turnover (INR. Crores)			
Net profit (INR. Crores)			
Net worth (INR. Crores)			

Note:

1. Submit the Audited balance sheet along with Profit & Loss Account for the financial year 2016-17, 2017-18 and 2018-19
2. Submit CA Certified Statement for the financial year 2016-17, 2017-18 and 2018-19 on the Net worth.

Annexure-F: BoQ Template

Sl. No.	Specifications		Item Code	Quantity	Units
1	**Category-A: Verification Solution**				
1.1	**Sub Category -A1: Logic Simulation Tool**				
1.11	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item1	240	licenses
1.12	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item2	8	licenses
1.2	**Sub Category -A2: Low power support**				
1.21	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item3	12	licenses
1.22	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item4	1	licenses
1.3	**Sub Category -A3: Formal Verification**				
1.31	1	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item5	1	licenses
2	**Category-B:Logic Equivalence Checking Solution**				
2.1	**Sub Category -B1: Logic Equivalence Checks**				
2.11	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item6	72	licenses
2.12	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item7	2	licenses
2.2	**Sub Category-B2: Low Power Logic Equivalence Checks**				
2.21	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item8	12	licenses
2.22	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item9	1	licenses
2.3	**Sub Category-B3: Logic Equivalence Check ECO flow**				
2.31	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item10	12	licenses
2.32	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item11	1	licenses

3	**Category-C: RTL Synthesis Solution**				
3.1	**Sub Category -C1: RTL Synthesis**				
3.11	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item12	48	licenses
3.12	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item13	3	licenses
3.2	**Sub Category-C2: Physically Aware Synthesis**				
3.21	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item14	48	licenses
3.22	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item15	3	licenses
3.3	**Sub Category-C3: Low Power Synthesis**				
3.31	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item16	12	licenses
3.32	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item17	1	licenses
4	**Category-D:Floorplanning, Partitioning Place & Route Solution**				
4.1	**Sub Category-D1: Floorplanning, Place and Route**				
4.11	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item18	84	licenses
4.12	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item19	4	licenses
4.2	**Sub Category-D2: Low Power Support**				
4.21	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item20	12	licenses
4.22	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item21	1	licenses
4.3	**Sub Category-D3 : Advance node features**				
4.31	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item22	42	licenses
4.32	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item23	2	licenses
5	**Category-E: Signoff Timing Solution**				
5.1	1	Countrywide floating monthly licenses usable for	Item24	84	licenses

		4 years with user flexibility for start date and end date of each license			
5.2	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item25	4	licenses
6	**Category-F: Signoff Power Solution**				
6.1	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item26	42	licenses
6.2	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item27	2	licenses
7	**Category-G: DFT & ATPG Solution**				
7.1	**Sub Category-G1 : DFT**				
7.11	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item28	12	licenses
7.12	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item29	2	licenses
7.2	**Sub Category-G2 : ATPG**				
7.21	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item30	12	licenses
7.22	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item31	2	licenses
7.3	**Sub Category-G3 : MBIST**				
7.31	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item32	6	licenses
7.32	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item33	1	licenses
7.4	**Sub Category-G4 : LBIST**				
7.41	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item34	6	licenses
7.42	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item35	1	licenses
8	**Category-H: Extraction & Physical Verification Solution**				
8.1	**Sub Category-H1 : RC Extraction**				
8.11	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item36	72	licenses

8.12	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item37	2	licenses
8.2	**Sub Category-H2 : DRC Verification**				
8.21	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item38	72	licenses
8.22	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item39	2	licenses
8.3	**Sub Category-H3 : LVS Verification**				
8.31	1	Countrywide floating monthly licenses usable for 4 years with user flexibility for start date and end date of each license	Item40	72	licenses
8.32	2	Countrywide floating perpetual licenses inclusive of 1 year AMC	Item41	2	licenses

Annexure-G: Tender Acceptance Letter

TENDER ACCEPTANCE LETTER

(To be given on Company Letter Head)

To: Date:

The Section Head (Purchase)
Centre for Development of Advanced Computing (C-DAC)
Vellayambalam, Thiruvananthapuram
Kerala-695033
Tel No.: 0471-2312672, 2723333

Dear Sir,

SUB: Acceptance of Terms & Conditions of Tender.

Ref: Tender Reference No

1. I/We have downloaded / obtained the tender document(s) for the above mentioned `Tender/Work' from the web site(s) namely: eprocure.gov.in as per your NIT / advertisement, given in the above mentioned website.

2. I/We hereby certify that I / We have read the entire terms and conditions of the tender documents (including all documents like annexure(s), schedules(s), etc.), which form part of the contract agreement and I / We shall abide hereby by the terms / conditions/ clauses contained therein.

3. The corrigendum(s) issued from time to time by your department / organization too has also been taken into consideration, while submitting this acceptance letter.

4. I/We hereby unconditionally accept the tender conditions of above mentioned tender document(s) / corrigendum(s) in its totality / entirety.

5. I/We do hereby declare that I / We have read and understood the entire technical specification laid down in the tender document and has prepared the technical bid in compliance with the technical requirements specified in the document.

6. I / We certify that all information furnished by the our Firm is true & correct and in the event that the information is found to be incorrect/untrue or found violated, then your department/ organization shall without giving any notice or

reason therefore or summarily reject the bid or terminate the contract, without prejudice to any other rights or remedy including the execution of Bid Securing Declaration / forfeiture of the full earnest money deposit absolutely.

7. I/We hereby declare that I/we would abide highest code of integrity in this procurement process and that I/we are aware that, in case of any transgression on our part in this regard, would entail removal of us from the list of registered suppliers, besides other punitive actions such as cancellation of contract, banning and blacklisting etc.

Yours Faithfully,

Authorized Signatory.

(Signature of the Bidder, with Official Seal)