Four Days C-DAC Internal Training Programme
on
Hybrid Computing: Co-processors & Accelerators – Case Studies
(Era of Multi-to-Many Core Processors)
at
C-DAC ACTS PUNE during *September 24-27, 2013*
OR
CMSD, University of HYDERABAD during *October 15-18, 2013*

Philosophy

Recognizing the evolving technology growth on ***multi-to-many core systems to solve Applications of C-DAC Projects,*** it is imperative for us to move up the value chain of technical training. In view of exposure to these areas is an essential and urgent requirement for our CDAC projects, our Director General **Prof. Rajat Moona** took initiatives and discussed with us to to take-up this internal technical training programme. The HPC-FTE group seeks to enhance the knowledge quotient of C-DAC technical staff through internal training on above areas. The objective is to ensure that C-DAC members will equip with excellent problem skills on latest "*Multi-to-Many-Core technologies for their Apps*" that are being used in their projects and produce outstanding IT professionals to meet the target deliverables of C-DAC IT projects.

I sincerely thank **Dr. Hemant Darbari** (Executive Director, C-DAC, Pune), **Dr. P.K.Sinha** (Senior Director Corporate R&D), **Mr. Aditya Sinha** (ACTS, Pune) & Corporate and C-DAC Staff for their continuous support to take-up this training programme.

In brief:

- *Staff from Pune, Mumbai, Delhi, Noida, Mohali, Kolkatta can attend **PUNE** Prog.*
- *Staff from Hyderabad, Chennai, Bengaluru, Thiruvananthapuram can attend **HYDERABAD** Prog.*
- *Maximum allowed participants from each centre is atmost six (6) & will include others, if possible.*
- *Participation is based on recommendation of Executive Director and HR dept. will co-ordinate.*
- *No registration fee is charged but the amount of expenditure per person to attend this training will be intimated to respective HR dept. The finance dept. of C-DAC participant centre should transfer the amount in coordination with their HR dept. after submission of invoice by training prog. Coordinator.*

For more details, please visit Page No. 2 and Page No. 3.

C-DAC Internal Training Programme for Tech. Staff (*)

CDAC-ITP-2013

C-DAC staff from Pune, Mumbai, Noida, Mohali, Kolkatta can attend

4-days Internal Training on

Hybrid Computing: Coprocessors & Accelerators – Case Studies

(Era of Multi-to-Many Core Processors)

***Venue*: C-DAC ACTS, Pune** **Schedule: September 24 –27, 2013**

Contact Email: cdacitp2013@cdac.in

(C-DAC-ITP-2013** is co-located with **hyPACK-2013)

hyPACK-2013

C-DAC staff from Hyderabad, Chennai, Bengaluru & Thiruvananthapuram can attend

4- days National Technology Workshop on

"**Hybrid Computing-Coprocessors & Accelerators-Power-aware Computing and Performance of App. Kernels (hyPACK –2013) "**

Jointly organized by C-DAC, Pune & CMSD, University of Hyderabad

***Venue:* CMSD, University of Hyderabad**; **Schedule: October 15 –18, 2013**

Visit: *http://www.cdac.in/hypack2013* **Contact email: *hypack2013@cdac.in***

C-DAC technical staff whose projects require programming & performance on "Multi-to-Many-Core Processors" can avail this opportunity. The interested C-DAC staff can be nominated by HR dept. of respective centre(s) in consultation with Centre Head or Executive Director. *No registration fee is charged but* HR dept of respective C-DAC Centre is required to co-ordinate with their finance department to pay the amount of expenditure for various services provided to the their own centre's participant to C-DAC-Pune, subject to workshop Coordinator submits in-voice after completion. The organizers will try their best to arrange accommodation facility in government aided institute guest-houses or service apartments or hotels. Each participant should pay his/her own accommodation charges as per tariff charges of their stay. The organizers provide break-fast, lunch and refreshments on all workshop days.

- Information about **C-DAC-ITP-2013** (Sep 24-27, 2013): Refer Page No. 3
- Information about **HYPACK-2013** (Oct 15-18,2013) Visit http://www.cdac.in/hypack2013/

Last Date for Registration for PUNE: September 20 , 2013
Last Date for Registration for Hyderabad: October 01, 2013

Participants are required to bring their OWN lap-top

 # Selection for participation is decided by HR dept &the Executive Director of C-DAC Centre.

C-DAC-ITP-2013 (Sep 24-27, 2013) : selected topics of given below will be covered.

50% Class-room lecture / 50% Lab. on Xeon-Phi & GPUs / Case Studies

Day-1 & Day-2:

- Programming on - Intel Xeon Phi Coprocessors multicore processor HPC Systems
- Xeon Phi usage model: MPI *versus* Offload; Compiler and Prog. Model; Approaches to Vectorization. Complier Directives; OpenMP-4.0, Intel TBB, Intel Cilk Plus, Intel MKL
- Intel Xeon-Phi Coprocessor Architecture; Coprocessor System software; Tuning Memory Allocation Perf., Huge Page Sizes; Profiling & Tuning Tools-
- Tuning & Performance Issues- Measurement of Power Consumption for App Kernels; External Power-Off Meter; Application Kernels; Energy Efficiency & Performance Issues

Day-3 & Day-4:

- HPC Cluster-NVIDIA GPUs and AMD GPUs /HPC Cluster with Accelerators
- An Overview of CUDA enabled NVIDIA GPUs : CUDA SDK/APIs; CUDA - Optimization & Performance Issues; Efficient use of different memory types, (CUBLAS, CUFFT, CULA Tools, MAGMA, CUSPARSE, Thurst); CUDA-OpenACC APIs; NVIDIA-OpenCL CUDA NVIDIA GPU Cluster - Kepler GPUs; NVIDIA CUDA – for Application Kernels on GPGPUs (NVIDIA KEPLER Features- Directives-OpenACC,OpenCL)
- An Overview of AMD Accelerated Parallel Processing (APP) Capabilities; AMD APUs - OpenCL Prog. On Multi-Core CPUs & Multi-GPUs; AMD APP Math libraries- BLAS & FFTs; AMD APP SDK, AMD tools- Aparapi APIs; AMD OpenCL tuning & performance; HPC AMD GPU Cluster: Host CPU (Pthreads, OpenMP, MPI) with OpenCL on AMD GPUs; Health Monitoring of GPU Cluster

An Overview of Hands-on:

- Memory Allocators, Software Threading, Mixed Programs (OpenMP 3.0/4.0, POSIX Threads, Intel TBB, MPI, Memory allocators) for Numerical (Dense/Sparse Matrix Comps.); & Non-Numerical Comps. Multi-Core Software tools; Application and System Benchmarks -Top-500 & HPC Challenge Benchmarks;
- Prog. on Intel Xeon Phi; MPI *versus* Offload; Compiler & Prog. Model; Prog. Paradigms - OpenMP, Intel Cilk Plus, Intel MKL; Tuning & Perf, Huge Page Sizes; Profiling
- Basic prog. (NVIDIA GPU Comp. CUDA 4.0 SDK & AMD GPGPUs - AMD-APP SDK); CUDA Toolkit; CUDA Matrix Comps. Lib,; OpenCL - NVIDIA - CUDA Prog. on Numerical Comps. CUDA Streams; Multi-GPU progs,; NVIDIA CUDA OpenACC - Prog.
- AMD-APP- OpenCL; OpenCL/CUDA -Multi-GPU; NVIDIA /AMD-APP Profilers & Tools; NVIDIA NVML APIs - Prog.; Measure Power-aware Perf. for application kernels
- CUDA /OpenCL Programs on Numerical Comps. (Dense /Sparse Matrix Comps.); Partial Diff. Eqs.; String Search Alg.; FFTs; Image Proc Alg. Prog, Environment on HPC GPU Cluster; Performance issues of Benchmarks & Application Kernels Mixed Prog. on Host CPU (MPI, OpenMP, Pthreads) and CUDA/OpenCL on devices, OpenACC, OpenMP 4.0.

Special lectures: Application Kernels & Case Studies

- Mixed Programming for Numerical /Non-Numerical Computations on multi-core Processors with Intel Xeon-Phi coprocessors, and NVIDIA /AMD GPU accelerators; Application & System Benchmarks & Performance; Image Processing Applications; Bio-Informatics – String Search Algorithms & Sequence Analysis; Dense / Sparse Matrix Computations on HPC Cluster with accelerators and Co-Processors; Solution of Partial Diff. Eqs. (FDM & FEM); FFT Libraries; Invited lectures on Information Sciences.