10G ETHERNET MAC IP CORE

INTRODUCTION

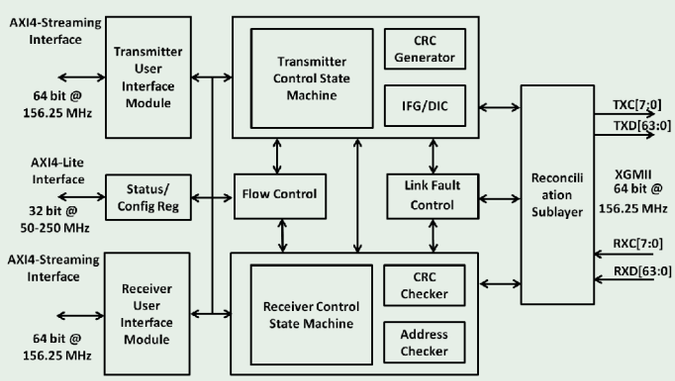
The 10GbE MAC core is compliant with IEEE802.3-2008 (802.3ae) specifications. The core is designed to support different configuration modes controlled by core's register file.

The 10GbE MAC core has a data path of 64 bits. The core has AXI4-Streaming user application interface. The application interface is designed as a 64-bit bus operating at 156.25MHz. The core also provides AXI4 - Lite interface to read/ write configuration registers for control and configuration of the 10GbE MAC.

CORE FEATURES

- Compliant with IEEE 802.3ae specification with preamble/SFD generation, frame padding, CRC generation and checking on transmit and receive respectively.
- XGMII interface operating at 156.25MHz.
- Implements Reconciliation Sublayer (RS) functionality with start and terminal control character alignment, error control character and fault sequence insertion and detection.
- Supports IEEE 802.3x XON-XOFF Pause Frame generation and termination for traffic flow control.
- Supports Deficit Idle Count (DIC) mechanism to maintain average 12 byte Inter Frame Gap (IFG).
- Padding of frames if the size of frame is less than 64 bytes.
- Performs Reconciliation Sublayer functionality by inserting proper control characters as specified by IEEE 802.3ae specifications.
- Automatic generation of FCS/PAD during transmission on per frame basis.
- Optional Forwarding of CRC to the user application interface.
- Status signals available with each frame on the user interface; providing information such as frame length, valid frame, address mismatch, CRC error etc
- Internal XGMII loop-back (Optional).
- Supports Jumbo frames.
- Configurable Transmit and Receive FIFOs.
- Provides AXI4-Streaming user application interface with 64-bit bus operating at 156.25MHz.
- Provides AXI4-Lite interface to read/ write configuration registers for control and configuration of the 10GbE MAC.
- Statistics counters indicating total number of valid frames, CRC errors and address check errors etc which can be reset by the user.
- 10GbE MAC IP core design has been tested and validated on Xilinx Virtex-6 HX380T FPGA device.

BLOCK DIAGRAM



Centre for Development of Advanced Computing (C-DAC)
A Scientific Society of the Ministry of Electronics and Information Technology, Govt. of India
C-DAC Knowledge Park, No. 1, Old Madras Road, Byappanahalli, Bengaluru 560 038, INDIA
Tel: +91-8066116400, **Fax:** + 91-80-2524 7724, www.cdac.in