High Speed Multi-lane LVDS Inter-FPGA Communication Link

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Abstract

As serial signal speeds approach 400Mhz and above, it is advised not to sign-off a Printed Circuit Board (PCB) layout designed with thumb rules and guidelines. The PCB traces connecting pins of Integrated Circuits behave like transmission lines at higher speeds. Due to RLGC parasitic effects, a high speed signal suffers losses and signal integrity is not maintained at the receiver. Since a poor quality signal at the receiver affects system performance and board re-spins involve enormous time and money, the response of an interconnection between a driver and a receiver to high speed signals must be predicted before the board is manufactured. This helps the layout designer to make modifications in the layout until the predicted behavior is acceptable to him. This is done by simulating a model of the signal path consisting of the driver, interconnection and receiver using an industry standard simulator like HSPICE. High speed drivers and receivers have user adjustable parameters like Pre-Emphasis and equalization to enable a high speed signal to traverse effectively along an interconnection. An interconnection includes the cables and connectors in the signal path in addition to PCB traces.

Device manufacturers supply HSPICE models of drivers and receivers in an encrypted form to protect their designs, while the transmission line model of the traces is extracted by a 2-D Fieldsolver. Connector and cable models are obtained from the vendors.

Cadence Allegro PCB SI provides the user an environment to assign models to the driver and receiver terminals of devices and extract the topology of an interconnect to be simulated. In order to use the manufacturer's encrypted models in the Cadence environment, they must first be wrapped into Cadence's native Device Modeling Language (DML) format.

This article describes the methodology to wrap these encrypted models to make them usable in the Cadence Design Environment for Signal Integrity Simulation. Here, we take the case of a high speed differential signal path consisting of driver and receiver models for RocketIO transceivers which are part of Xilinx Virtex-4 Field Programmable Gate Arrays (FPGA). The encrypted HSPICE models are available to Xilinx customers. These models are wrapped into an IbisIOCell as DML macromodels using the text editor of the Model Integrity tool. Any errors reported by the parser are corrected. The model is then tested in SigXplorer and assigned to the driver and receiver pins. IbisDevice and PackageModels are also created as required by the DML syntax and the complete model is assigned to the FPGA device. The topology of the high speed signal path can now be extracted into SigXplorer. The HSPICE netlist is then generated, which is submitted to the HSPICE simulator.