

# Floating Point Matrix Multiplication on a Reconfigurable Computing System

Sajish C<sup>1</sup>, Yogindra Abhyankar<sup>1</sup>, Shailesh Ghotgalkar<sup>1</sup>, K. A. Venkatesh<sup>2</sup>  
<sup>1</sup>Hardware Technology Development Group  
Centre for Development of Advanced Computing, Pune 411 007, India.  
<sup>2</sup>Alliance Business Academy, Bangalore 560 076, India.  
Email: [yogindra@cdac.in](mailto:yogindra@cdac.in)

## Abstract:

*Matrix multiplication is one of the most fundamental and computationally intense operation that is used in a variety of scientific and engineering applications. There are many implementations of this normally  $O(n^3)$  operation. These implementations differ mainly in terms of algorithms or the platforms. In this paper we present our experimentation of using a reconfigurable computing platform for calling such a routine. This routine use our own developed IEEE-754 compliant double precision hardware library elements implemented on our own developed FPGA based reconfigurable platform to provide acceleration.*