Co-simulation: Verification Advantage with PCI Express Endpoint SystemC Model

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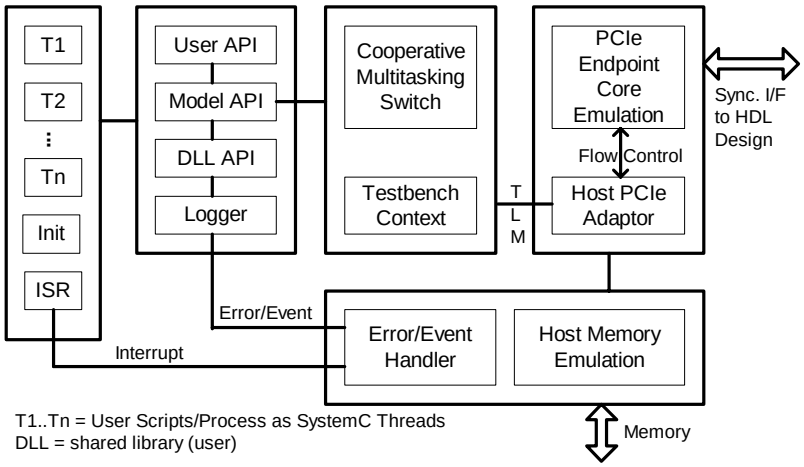
Abstract

Functional verification of a Network Processor design requires a simulation environment that emulates a generic host-system. The emulation involves multiple processors, direct memory access, interrupt service routines (ISR), exceptions and error handling, synchronization objects, etc. Additionally, the Network Processor (providing the transport layer) specific driver support involves special data-structures, programmed I/O, block memory transactions. Our design of Network Processor, in Hardware Description Language (HDL), uses PCI Express (PCIe) interconnect module (an Endpoint core from third-party). We have developed a replacement simulation-model using restricted-use of SystemC (to improve simulation speed). Besides these requirements, its additional aim was to reduce overall simulation speed bottlenecks, simplify testbench creation (independent of programming language, e.g. C/C++), integrate testbench module within the design itself (by replacing Endpoint Core, and concentrate not on testbench creation but on testcases). The high-level architecture of the model is shown below.



This eliminates the need for two back-to-back instances of PCIe Endpoint Cores and additional testbench creation in HDL. The improved overall simulation speed (by factor of ~10) and reduced memory usage (by factor of ~5.5) results are quite encouraging to apply same model to verify other designs having similar interconnect. The testbench complexity was transferred from HDL to external processes enabling efficient test-suite development for simulation.

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