CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING
A-34, PHASE VIII, INDUSTRIAL AREA, MOHALI
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SUMMER TRAINING (6 WEEKS) – 2024

VLSI Design & FPGA Implementation

DAY	THEORY	PRACTICAL
	WEEK - 1	
1	Introduction to Digital Design	Introduction to EDA Tools
2	Digital Design-1	Design Entry Tools
3	Digital Design-2	Simulation Tools
4	Digital Design-3	Lab- Exercise
5	Finite State Machine concepts	Lab- Exercise
	WEEK - 2	
6	Introduction VLSI Design flow	Test-1
7	Introduction to VHDL	Lab- Exercise
8	Various Modeling styles	Lab- Exercise
9	Data types	Lab- Exercise
10	Data types /VHDL statements	Assignment-1
	WEEK - 3	
11	VHDL Modeling of Combinational circuits- 1	Lab- Exercise
12	VHDL Modeling of Combinational circuits -2	Lab- Exercise
13	VHDL Modeling of sequential circuits – 1	Lab- Exercise
14	VHDL Modeling of sequential circuits – 2	Lab- Exercise
15	Basic of Verilog HDL Languages	Lab- Exercise
	WEEK - 4	
16	FSM based Modeling of Digital Circuits	Lab- Exercise
17	Introduction to: Full-Custom, Semi-Custom Design	Introduction to Xilinx FPGA Kit
18	FPGA Based Design Flow	Lab- Exercise
19	Introduction to TCAD Simulation Tools.	Lab- Exercise
20	Device Simulation using TCAD	Lab- Exercise
	WEEK - 5 & 6	
Project: Design and Implementation of a Digital Circuit and Electronic Devices In the mid of 6th week each student will submit a project report which will be having significant contribution in total grading for the training.		

Duration: 6 Weeks (3 Hours per day)

Eligibility: B.E /B.TECH. (ECE/EEE/EE) 2nd or 3rd Year Students

Fee: As per C-DAC Norms