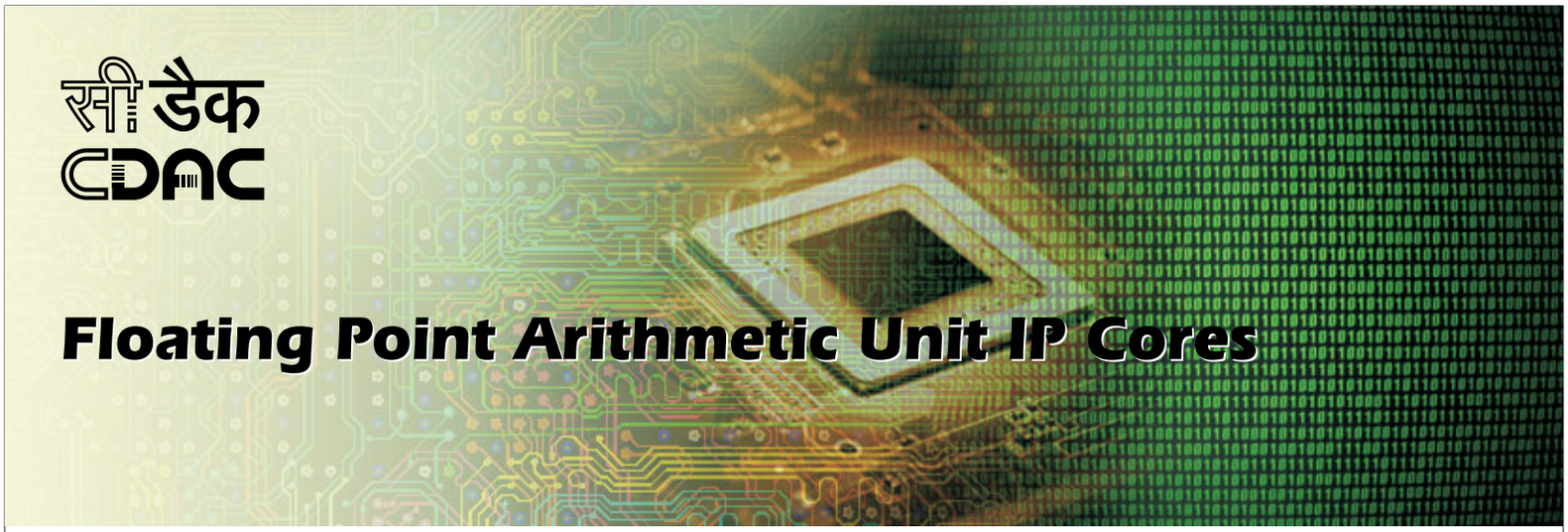

# Floating Point Arithmetic Unit IP Cores

## INTRODUCTION

Floating Point (FP) computations play a significant role in a variety of scientific and engineering applications. The FPU arithmetic core can be used in applications such as: climate modelling, supernova simulations, electromagnetic scattering theory, Computational Geometry and Grid Generation to image processing, FFT calculation, matrix arithmetic, Eigen value calculation, Jacobi solver, etc.

The FP arithmetic IP cores are available in two variants viz. co-processor compatible with RISC-V* ISA and accelerator with custom op-codes.

## KEY FEATURES OF BOTH VARIANTS

- Supports operations like add/subtract, divide, square root, fused multiply-accumulate, comparison, conversion between floating point to fixed point and vice versa, logarithm (natural and base 10) and exponentiation.
- Fully compliant with IEEE-754 2008** standard for floating point.
- Support for both single and double precision data.
- Supports all special inputs like sNaN, qNaN, +Infinity and –Infinity, +zero, -zero.
- Handles all five exceptions like overflow, underflow, invalid, inexact and divide by zero.
- It also supports five different rounding modes as per IEEE-754 2008
- Optimized for performance (throughput) and latency.
- Fully synchronous design.
- Extensively validated and verified.
- Verified with software implementation for 2 million input operands as test cases.
- Verified with standard IBM test suite.
- Designs are tested on Virtex 6 FPGA.

## RISC-V FLOATING POINT INSTRUCTIONS SET ENABLED CO-PROCESSOR

- Compatible with RISC-V instruction set
- Supports 56 RISC-V Floating point operations
- Supports arithmetic, fused multiply accumulate, conversion, comparison, minimum/ maximum, movement, sign injection, flag operations
- Out-of-order execution and in order commit
- Moderately pipelined
- Developed using Bluespec system Verilog*** (BSV)
- Available as BSV source code and generated synthesizable Verilog code

## FP ARITHMETIC UNIT ACCELERATOR WITH CUSTOM OP-CODES

- FPU for high performance applications
- Deeply pipelined
- Supports 22 generic floating point operations
- Supports addition, multiplication, division, square-root, logarithm, comparison, signed/unsigned integer to floating point, floating point to signed integer, single precision to double precision conversion operations
- Custom defined op-codes for operations
- Developed using VHDL/Verilog RTL description languages
- Single and multiple concurrent FPU cores for data parallel HPC applications

## REFERENCES


* RISC-V – The Free and Open RISC Instruction Set Architecture, https://riscv.org/

** IEEE Standard for Floating-Point Arithmetic,http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=4610935

*** Bluespec Technologies and Solutions, http://www.bluespec.com/



**Centre for Development of Advanced Computing (C-DAC)**
**A Scientific Society of the Ministry of Electronics and Information Technology, Govt. of India**
C-DAC Knowledge Park, No. 1, Old Madras Road, Byappanahalli, Bengaluru 560 038, INDIA
**Tel:** +91-8066116400, **Fax:** + 91-80-2524 7724, www.cdac.in