Trinetra HPC Network

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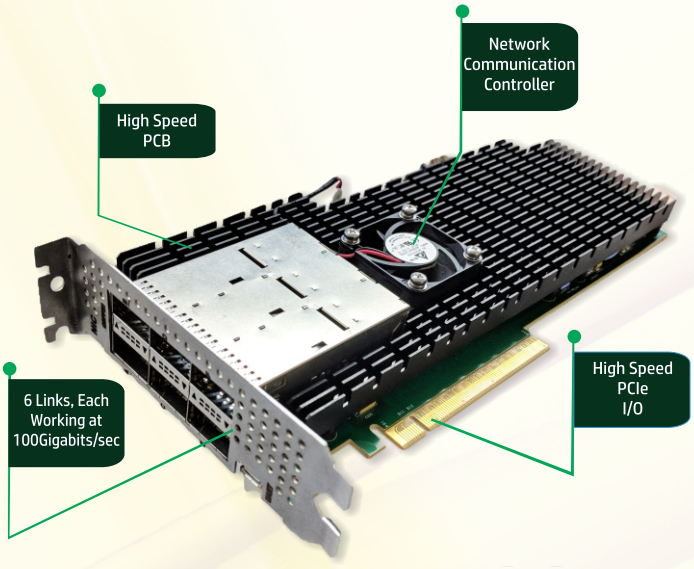
Paving the way towards Indigenous Exascale systems



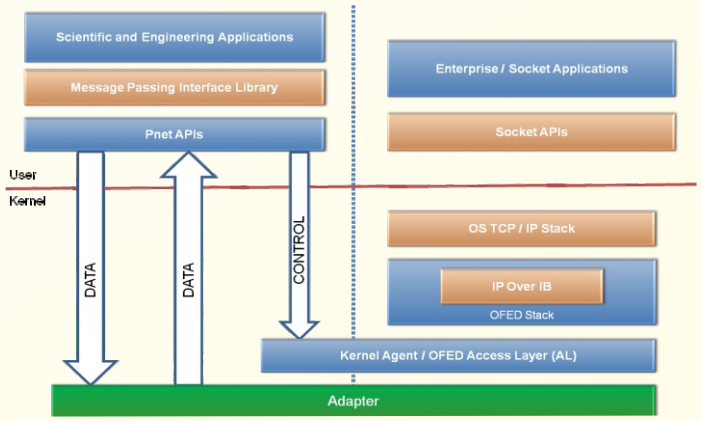
Trinetra-A Platform: 100Gbps, 6 links, 3D Torus topology

Key Features

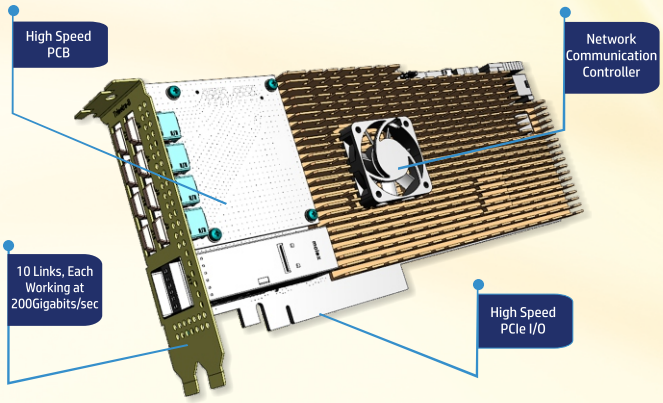
- High Bandwidth, Low latency implementation using innovative hardware capabilities, supported by lightweight software stack
- Design Drivers: 'Real' (User level) performance, Scalability, Power, Experimentation
- Handholding with Application Developers for optimal hardware/ software performance
- 3D Torus (Trinetra-A) and Dragonfly (Trinetra-B) topology for large scale scalability without dedicated switches
- Support for Multiple Processor and Platform Architectures
- Supports industry standard HPC programming (MPI) and Legacy (Sockets) interfaces
- Fourth Generation PARAMNet

Components

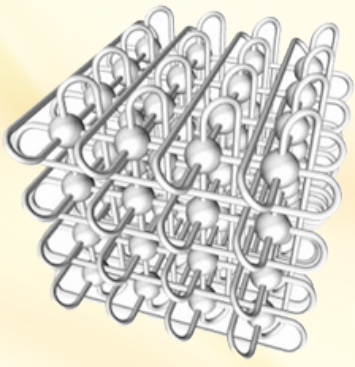
- Network Controller Chip (NCC) as VLSI chip implementation
- Platform supports multiple physical layer interfaces, allowing for Torus/Torus Derivative Topologies
- System software components (Device drivers, kernel/User components)
- OFED support
- HPC and Enterprise/Socket application support



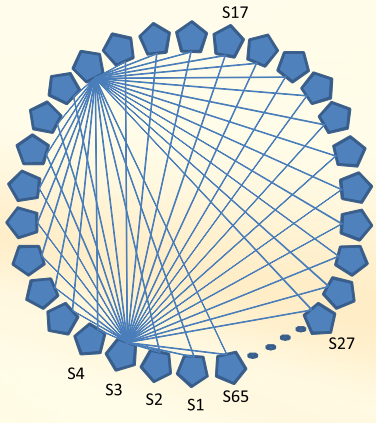
Software Stack



Trinetra-B Platform: 200 Gbps, 10 Links, Cascaded Hypercube Topology



3D Torus Topology



Dragonfly topology