Invitation for Expression of Interest (EoI) for Transfer of Technology (ToT) of Field-Programmable Gate Array (FPGA) Board

CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING
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1. Introduction

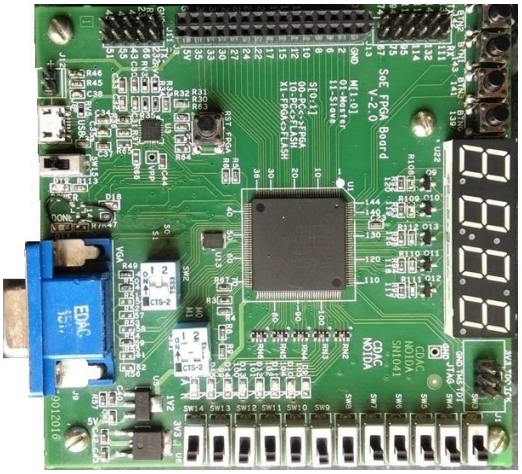
1.1. Brief history about C-DAC:

Centre for Development of Advanced Computing (C-DAC) is a premier R&D organization of the Ministry of Electronics and Information Technology (MeitY) mandated to carry out R&D in Information and Communication Technologies, Electronics (ICT&E) and associated areas. Although C-DAC was established with a clear mandate of R&D in high performance computing in 1988, over the last three decades, it has diversified into several other areas of ICT to respond to the needs of the society. With the zeal to convert its R&D outcomes into usable technologies, it is today a significant IT player with many innovative products and solutions. In addition, C-DAC has played a key role in IT education to fulfill the higher ICT education requirements of the country's IT industry.

1.2. About FPGA Board

1.2.1 Key features of the "FPGA Board"

The developed platform is an easy to use low-cost FPGA development board featuring Xilinx Spartan-6 FPGA. It is specially designed for facilitating the students and faculty to experiment with the concepts of system design using FPGAs. The board offers a rich set of features that make it suitable for use in the following areas:



- Laboratory for undergraduate courses,
- Variety of design projects,
- Development of sophisticated digital systems.

By default the board is powered from a +5V supply from USB cable. Built around a Xilinx Spartan-6 FPGA the board provides, a complete ready-to-use hardware suitable for hosting circuits ranging from basic logic devices to complex controllers. A large collection of on-board I/O devices/interfaces and all required FPGA support circuits are included, so countless designs can be created without the need of any other components. The design can be controlled and

configured through PC using high speed USB interface provided on the board. The board is designed to work with the free ISE WebPack software from Xilinx.

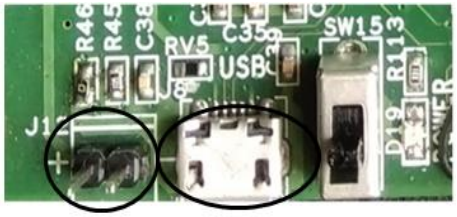
Main Features

- The Spartan 6 LX4 is optimized for high performance logic and offers:
    - 600 slices, each containing four LUTs and eight Flip Flops
    - 216 Kb fast Block RAM
    - Two CMTs (two DCMs and one PLL)
    - 8 DSP48A1 slices
- SPI Flash ROM that stores FPGA configuration indefinitely
- 25 MHz oscillator frequency
- USB cable for providing power and programming interface
- 8 LEDs, 4 Push buttons, 12 slide switches
- 4 digit seven segment display
- 8 bit VGA display
- UART communication pins
- 30 pin expansion connectors

1.2.2 Key Benefits of the "FPGA Board"

- Low Cost
- Simple hardware
- User friendly programmer
- Onboard peripherals to perform digital design experiments
- 30 pin expansion connectors for external digital I/O interface
- Students can perform various experiments ranging from combinational to sequential circuits
- Instructional material with step by step programming for a set of experiments is provided online
- Free access to e-learning content

1.2.3 Technical Specifications of the "FPGA Board" Power



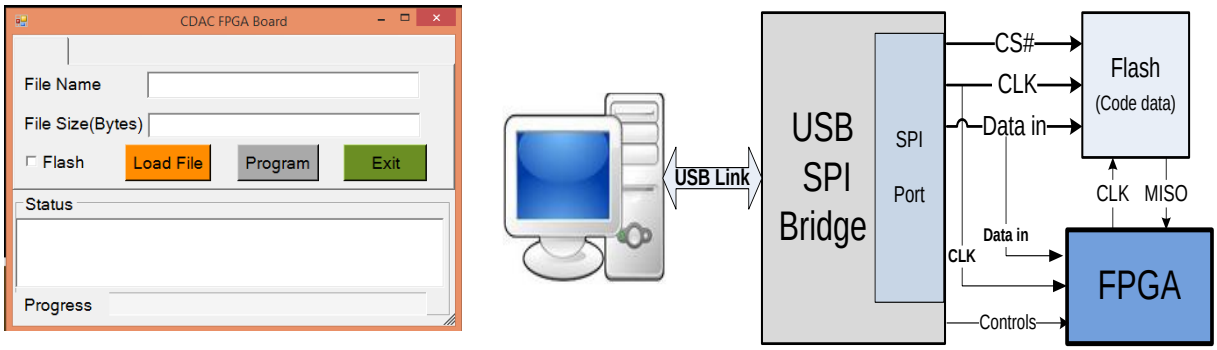
The FPGA board is typically powered from a USB cable, but a battery connector/dc power supply connector is also provided so that external supplies can be used. To use USB power, simply attach the USB cable. Voltages higher than 5V on either power connector may cause permanent damage.

Input power is routed through the power switch (SW15) to the 30-pin expansion connectors, to 800mA low dropout positive voltage regulator LD1117/12 voltage regulator and 1.0A Low dropout positive voltage regulator NCP1117/33. The NCP1117/33 produces the main 3.3V supply for the board. The LD1117/12 produces 1.2V supply voltage required by the FPGA. Total board current is dependent on FPGA configuration, clock frequency, and external connections. Required current will increase if larger circuits are configured in the FPGA, or if peripheral boards are attached.

Configuration

The FPGA board has an on-board USB to SPI controller which facilitates easy reprogramming of on-board SPI flash and FPGA through USB interface. The controller receives bit stream from the host application PC, programs it in to the SPI Flash and lets the FPGA boot from the flash.

The USB 2.0 interface provides fast and easy configuration download to the on-board SPI flash. Here we don’t need a programmer or special downloader cable to download the bit stream to the board. The FPGA can be configured in master or slave select modes. The device can also be configured and debugged using JTAG programmer. JTAG connector provides access to FPGA's JTAG pins. A XILINX platform cable can be used for JTAG programming. Figure shown below depicts the configuration interface connections.



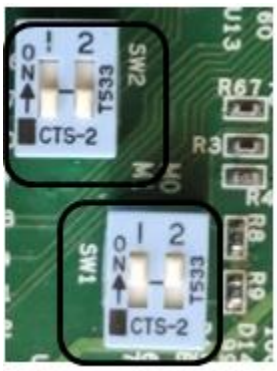
After power-on, the FPGA on the development board must be configured before it can perform any useful functions. During configuration, a "bit" file is transferred into memory cells within the FPGA to define the logical functions and circuit interconnects. The free ISE/WebPack CAD software from Xilinx can be used to create bit files from VHDL, Verilog, or schematic-based source files.

C-DAC's PC-based program called CLR13.0 can be used to configure the FPGA with any suitable bit file stored on the computer. The CLR13.0 uses the USB cable to transfer a selected bit file from the PC to the FPGA. CLR13.0 can also program a bit file into an on-board non-volatile ROM called "SPI Flash". Once programmed, the SPI Flash can automatically transfer a stored bit file to the FPGA at a subsequent power-on or reset event. The FPGA will remain configured until it is reset by a power-cycle event. The SPI Flash ROM will retain a bit file until it is reprogrammed, regardless of power-cycle events.

The following are the switch configuration for the FPGA board for configuring the FPGA chip:

SW1: 01- FPGA will act as a master to the Flash
11-When programming through PC, FPGA will be act as slave

SW2: 00-PC to FPGA programming
10-PC to Flash
X1-FPGA to Flash/ Flash to FPGA



To program the development board, attach the USB cable to the board. Start the CLR13.0 programmer and use the load file function to associate the desired bit stream file with the FPGA, or with the SPI Flash. Select the “Program” function for configuring the FPGA directly from the PC. Tick “Flash” function check box if you want to store data to the SPI Flash. The configuration file will be sent to the FPGA or SPI Flash, and the software will indicate whether programming was successful. The “Status LED” LED (D17) will glow, after the FPGA has been successfully configured.

Oscillator

The development board includes a primary Silicon Labs 501JAA25M0000BAG CMEMS oscillator that produces 25 MHz.

User I/O

Four pushbuttons and twelve slide switches are provided for circuit inputs. Pushbutton inputs are normally low and driven high only when the pushbutton is pressed. Slide switches generate constant high or low inputs depending on position. Pushbuttons and slide switches all have series resistors for protection against short circuits (a short circuit would occur if an FPGA pin assigned to a pushbutton or slide switch was inadvertently defined as an output).

Eight LEDs and a four-digit seven-segment LED display are provided for circuit outputs. LED anodes are driven from the FPGA via current-limiting resistors, so they will illuminate when logic '1' is written to the corresponding FPGA pin.

The development board uses 10 FPGA signals to create a VGA port with 8-bit color and the two

standard sync signals (HS – Horizontal Sync, and VS – Vertical Sync). A video controller circuit must be created in the FPGA to drive the sync and color signals with the correct timing in order to produce a working display system.

The FPGA board has two serial communication pins – the receiver, RX for receiving the data and the transmitter, TX for sending the data. The RX pin of the FPGA board should be connected to the TX of the other device with which one wants to communicate. Similarly, the TX pin of the FPGA board will be connected to the RX of the other device for the serial communication.

The development board provides 30-pin peripheral module ports. It provides 5V, 3.3V and two signals. Several module boards/devices can be interfaced to the board through these pins. For example A/D converters, speaker amplifiers, microphones, sensors etc.

1.3 Current status of FPGA board

The FPGA board developed by C-DAC has been tested for error-free functionality conforming to the highest industry standards. It is ready for mass production as an excellent low-cost option for students pursuing careers in Electronics R&D and manufacturing.

1.4 List of deliverables

The Design Document i.e. Schematic & Layout Gerber file and User Manual would be made available to selected vendor(s) after finalization of the tender which would be floated after processing this EoI.

2. Scope of Work

C-DAC intends to provide its FPGA solution to interested companies/vendors with good experience in development & deployment of PCB electronic boards. C-DAC, as a part of its R&D initiative and responsibility of supporting the Electronics industry is eager to proliferate this product in the market in collaboration with suitable industry partners.

3. Extent of Work

Expressions of Interest (EoI) are invited from interested companies/vendors engaged in electronics equipment manufacturing for Transfer of Technology of FPGA Board.

4. Documentation

C-DAC will provide detailed documentation for all sub-systems as per scope of work.

5. Training

C-DAC will impart orientation training about the functionality of FPGA Board through an elementary course.

6. Expression of Interest

C-DAC invites Expression of Interest bids in the format given in Annexure I (A & B).

6.1. Processing Fee

Processing fee of Rs. Ten Thousand only (Rs 10000/-) must be submitted by Demand Draft / Pay Order of any Scheduled Bank drawn in favor of C-DAC NOIDA. No Bank Guarantee towards Processing Fees will be acceptable. Processing Fees is non-refundable. Bids received without processing fee will automatically be rejected.

6.2. Validity of the EoI

The EoI bid submitted by the bidder will be valid for 180 days from the last date of submission of the bid.

6.3. Pre-bid Meeting/ Clarifications

6.3.1. A Pre-bid meeting of all the Bidders will be convened as follows:

Date of pre-bid Meeting: 4th Dec, 2017

Timing of pre-bid Meeting: 10:30 a.m.

Venue: Conference Hall, Academic Block, C-DAC, B-30, Sector - 62 NOIDA-201309

6.3.2. After deliberations in the pre-bid meeting, if found necessary, the queries along with the answers/clarifications will be sent to all prospective bidders.

6.4. Documents to be enclosed with EoI

6.4.1 List of documents:

- **a.** Bid Form containing complete details such as company name, address, etc. as per Annexure I A.
- **b.** Vendors Disclosures to support the various clauses in the eligibility criteria as per Annexure I B.
- **c.** Authority letter to designate a person interacting with C-DAC.
- **d.** Covering letter

6.4.2 Processing Fee

6.5. Bid Submission

The bid is to be submitted in a sealed cover containing two separate envelopes as explained below:

6.5.1. Envelope A: It should contain all the documents listed as para 6.4.1. The outer cover should mention "**Envelope A**-Documents only".

6.5.2. Envelope B: It should contain the processing Fee. The outer cover should mention "**Envelope B**- Processing Fees". This envelope must contain a Demand

Draft in favor of C-DAC NOIDA for Rs. 10,000/- (Rupees Ten thousand only, non-refundable) which will be considered as processing fees. Bids received without processing will automatically be rejected. No bank Guarantee will be acceptable in lieu of bank draft.

Put both envelopes; A and B inside a common envelope.

Address to;

"Bid for FPGA Board Technology Transfer"

"Dr. Arti Noor, Group Coordinator (Academics),
Centre for Development of Advanced Computing (C-DAC),
B-30, Academic Block, Sector – 62,
NOIDA - 201309".

It must be submitted **by 18th Dec 2017, 5 PM. Bids received later than this schedule will not be opened and will be returned to the bidders as received.**

6.6. Opening of Bids

The bids will be opened as per the following schedule:

i. **Date**: 19th Dec, 2017

ii. **Time**: 10:30 a.m.

iii. **Place:** Conference Hall, Academic Block, C-DAC B-30, Sector - 62 NOIDA - 201309

In case of any change in this schedule, participating bidders will be informed through e-mail at least three working days prior to convening such a meeting.

6.7. Selection Criteria

6.7.1. The bids will be opened by a duly designated committee on the given date and time in the presence of all bidders.

6.7.2. After opening the bids, Envelope B will be opened first and scrutinized to ascertain that the Processing Fee is in order.

6.7.3. Envelope A will be opened only in those cases where Processing Fee submitted in Envelope B is found to be in order.

6.7.4. A duly designated C-DAC committee will evaluate the documents submitted in envelope "A" for its completeness by having a preliminary scrutiny of the documents and as per the Eligibility Criteria as mentioned in Annexure I B.

6.7.5. Participating bidders will be informed after approval of the Committee's Evaluation Report in due course by C-DAC.

6.7.6. A panel of shortlisted vendors will be formed and all such shortlisted vendors will be authorized to participate in the final Tender.

6.7.7. Bidders are not supposed to have any interaction with the Committee members. However, C-DAC may seek clarifications from the bidders on the already submitted information.

6.8. Brief Terms & Conditions of the next stage of the Tender

6.8.1. Shortlisted Vendors are encouraged to sit with the FPGA development team of C-DAC at C-DAC NOIDA premises to understand the solution.

6.8.2. C-DAC will issue a letter in the form of a tender document to the short listed bidders giving out the license fees (as on point no. 7) & payment options and draft terms of the agreement.

6.8.3. Signing of vendor agreement between C-DAC and selected bidders(s). The

content and Terms & Conditions shall be ratified by the C-DAC Committee before signing by the Parties.

6.8.4. Telephone & e-mail support will be provided by C-DAC Noida FPGA team to the vendors for development of FPGA board for up to 6 (six) months at no extra cost.

6.9. Instructions to the Bidders

6.9.1. The information to be furnished for Expression of Interest is given in Annexure- I. Interested parties can submit the EoI along with Annexure-I (A & B) duly filled in with all relevant supporting documents as mentioned there-in. The vendors will be shortlisted based on the information furnished in Annexure I and assessment by the C-DAC committee.

6.9.2. A Pre-bid meeting of all the Bidders will be convened as per para 6.3. The purpose of this meeting will be to clarify the requirements as envisaged by C-DAC and also to address the queries, if any.

6.9.3. The EOI's submitted should be sealed properly as per para 6.5.

6.9.4. C-DAC may at its discretion, extend the deadline for the submission of EoI by amending the EoI documents in which case, all rights and obligations of C-DAC and bidders previously subject to the deadline will thereafter be subjected to the deadline as extended.

6.9.5. To assist in the examination, evaluation and comparison of EoI, C-DAC at its discretion can ask the bidder for the clarification of its EoI. The request for clarification and the response shall be in writing. However no post submission of EoI, clarification at the initiative of the bidder shall be entertained. C-DAC reserves the right to visit the facilities of the bidders if required.

6.9.6. Bidders if they choose, may prior to submitting their Expression of Interest, visit

C-DAC with prior appointment.

6.9.7. Bidders may be called for making a presentation before the C-DAC committee.

6.9.8. C-DAC representatives may visit bidder's facilities for assessment.

6.9.9. C-DAC will issue Tender Documents to short-listed bidders for the submission of financial bids.

6.9.10. At any time before the submission of EoI, C-DAC may carry out amendment(s) to this EoI document and/or the schedule. The amendment will be made available on the website (www.cdac.in) and will be binding on all bidders. C-DAC authorities may, at their discretion, extend the deadline for the submission of proposals in such a case.

6.9.11. C-DAC authorities reserve the right to accept or reject any application without assigning any reason thereof.

6.9.12. Bids that are incomplete in any respect or those that are not consistent with the requirements as specified in this document or those that do not adhere to formats wherever specified may be considered non-responsive and may be liable for rejection and no further correspondence will be entertained with such bidders.

6.9.13. Canvassing in any form would disqualify the applicant.

6.9.14. The bidder must sign on each page of the bid document submitted as a token that all terms and conditions reflected therein have been fully understood.

6.9.15. Any willful concealment of facts by the bidder, if detected at any stage of the tender processing, will lead to the rejection of the bid.

6.9.16. All the documents submitted in response to this EoI must be properly bonded. No loose document should form a part of the bid. Each page must have a footer containing the information on the pages as per the format "Current Page Number / Total number of pages". All these pages must be signed.

6.9.17. Preferably there should not be any over-writing. However, any corrections must be initialed by the authorized person.

6.9.18. C-DAC reserves the complete right to cancel the EoI process and reject any or all of the bids at its sole discretion.

7. License fee: Rs 50000/- (Rs Fifty thousand) one time only. This fee will be paid by successful bidders in the form of a demand draft in favor of C-DAC payable at Noida/Delhi.

8. For any clarifications on the Expression of Interest document or application process, please contact Mr. Ravi Shankar Rai (email – ravishankarrai@cdac.in Mob: 9968836506) & Dr. Sunita Prasad (email – sunitaprasad@cdac.in Mob: 9810827982)