Expression of Interest (EoI) for Transfer of Technology

PARAMETRIZED POSIT ARITHMETIC UNIT IP CORE

(RISC-V Instruction Set Architecture Enabled)

Issued by

Centre for Development of Advanced Computing

(A Scientific Society of the Ministry of Electronics and Information Technology, Govt. of India)

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Invitation for Expression of Interest (EoI) for Transfer of Technology (ToT)
Instructions to the Bidders to be provided by C-DAC

Applications are invited for the purpose of Technology Transfer/commercialization of Parametrized Posit Arithmetic Unit IP (RISC-V Instruction Set Architecture Enabled) core from the organizations with relevant experience.

1. The information to be furnished by the bidders is given in Annexure-I. Interested parties can submit the EOI along with Annexure-I (Part A & B) duly filled in with all relevant supporting documents as mentioned in Para 3.0 of EOI document.

2. Pre-bid Meeting: A Pre-bid meeting of all the Bidders will be convened on **27th April 2022** at our office address mentioned above or Online. The purpose of this meeting will be to clarify the requirements as envisaged by C-DAC and also to address the queries if any. Due to Covid-19 protocols, the bidders can also send their queries at least two days prior to the date of pre-bid meeting to the Email ID: aswath@cdac.in. The clarifications against the queries received will be hosted in our website www.cdac.in. The link to join Online meeting will be informed upon request for joining and submission of queries, doubts, clarifications etc., if any.

3. The EoI's submitted should be sealed properly and marked "EoI for ToT of Parametrized Posit Arithmetic Unit IP core" so as to reach the following address on or before on **30th May 2022 @ 3.00 pm.**

   The Executive Director
   Centre for Development of Advanced Computing (C-DAC)
   No.1, Old Madras Road, Byapannahalli,
   Bangalore – 560 038.
   Phone No: 080-25093400
   Fax No: 080-25247724

   The EoI bids shall be opened on **30th May 2022 @ 3.30 pm**

   C-DAC, Bangalore may at its discretion – extend this deadline for the submission of EoI by amending the EoI documents, in which case all rights and obligations of C-DAC, Bangalore and bidders previously subject to the deadline will thereafter be subjected to the deadline as extended.

4. To assist in the examination, evaluation and comparison of EoI, C-DAC, Bangalore at its discretion can ask the bidder for the clarification of its EoI. The request for clarification and the response shall be in writing. However no post submission of EoI, clarification at the initiative of the bidder shall be entertained. C-DAC, Bangalore reserves the right to visit the facilities of the bidder if required.

5. Bidders if they choose, may prior to submit their Expression of Interest, visit C-DAC, Bangalore with prior appointment with the contact person as stated below.

6. Bidders may be called for making a presentation before the Technology Transfer Committee.

7. The official(s) of C-DAC, Bangalore may visit bidder's facilities for the assessment.
8. C-DAC, Bangalore will issue tender documents to short-listed bidders for the submission of financial bids.

9. At any time before the submission of EoI, C-DAC, Bangalore may carry out amendment(s) to this EoI document and/or the schedule. The amendment will be made available on the website (www.cdac.in) and will be binding on them. The Authority may at its discretion extend the deadline for the submission of proposals.

10. C-DAC, Bangalore reserves the right to accept or reject any application without assigning any reason thereof.

11. Bids that are incomplete in any respect or those that are not consistent with the requirements as specified in this document or those that do not adhere to formats, wherever specified may be considered non-responsive and may be liable for rejection and no further correspondences will be entertained with such bidders.

12. Canvassing in any form would disqualify the applicant.

13. For any clarifications on the Expression of interest document, the following may be contacted through e-mail/FAX/Letter:

Details of the contact person

For Technical Queries:
Shri. Vivian Desalphine, Associate Director, SHVD Group **or**
Shri. Aneesh Raveendran, Principal Technical Officer, SHVD Group.
Centre for Development of Advanced Computing,
No.1, Old Madras Road, Byapannahalli,
Bangalore – 560 038.
Phone No.: +91-80-25093425, 25093428
Fax No. 080-25247724
Email: viviand@cdac.in, raneesh@cdac.in

For EOI-Tender Queries.
Shri. Aswath Rao S,
Senior Purchase Officer, PS&O,
Centre for Development of Advanced Computing,
No.1, Old Madras Road, Byapannahalli,
Bangalore – 560 038.
Landline: +91-80-25093462
Fax No. 080-25247724
Email: aswath@cdac.in

Competent authority
C-DAC, Bangalore.

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1. Introduction

Secure Hardware and VLSI Design Group (SHVD) of C-DAC, Bangalore has indigenously designed and developed Parametrized Posit Arithmetic Unit IP core, which is RISC-V Instruction Set Architecture enabled, and the technology is available for transfer to interested establishments. C-DAC, Bangalore would like to invite competent industrial partners, for commercialization of the RISC-V ISA enabled Parameterized Posit Arithmetic IP core through transfer of technology.

2. About C-DAC

Centre for Development of Advanced Computing (C-DAC) is a premier R&D organization under Ministry of Electronics and Information Technology (MeitY), for carrying out R&D in IT, Electronics and associated areas. Different areas of C-DAC, had originated at different times, many of which came out as a result of identification of opportunities. More details about C-DAC can be found at www.cdac.in.

3. About RISC-V Instruction Set Architecture Enabled Posit Arithmetic Unit IP Core

Description

The parameterized Posit Arithmetic Unit IP core designed by C-DAC, Bangalore is compliant with Posit arithmetic specifications. The Posit IP arithmetic/core is treated as an alternate for IEEE 754-2008 compliant Floating-Point standard/core. The core is designed to support parameterized N and ES values. Also, it supports RISC-V ISA enabled operations with half (P16), single (P32) and double (P64) precision Posit numbers with various rounding modes. Posit IP core is compatible with RISC-V Instruction Set Architecture extensions F and D and has the interfaces to integrate the Posit Arithmetic Unit to a pipelined RISC-V microprocessor.

The developed Posit Arithmetic Unit IP core is RISC-V Instruction Set Architecture enabled. The IP supports 96 instructions, which are floating point instructions specified in RISC-V Instruction Set Architecture Version 2.2. Half, single and double precision Posit modules are fused together to reduce the number of functional units (total functional units are 7). The Posit IP core supports operations such as addition/subtraction, multiplication, division, comparison, conversions (Posit to integer, integer to Posit, and Posit to Posit). Posit Arithmetic Unit IP core is synthesized targeting Virtex Ultrascale VCU118 FPGA development board, operating at 125MHz, using Xilinx Vivado software.

The Key features of Posit Arithmetic Unit IP core:

- Compliant with Posit arithmetic specifications.
- Developed using Verilog HDL.
- RISC-V Instruction Set enabled (ISA version 2.2).
- Supports 96 RISC-V FP instructions (Single and Double Precision FP instructions).
- Supports half, single and double precision Posit operations.
- Fused modules for Posit operations.

- Supports 5 rounding modes: Round toward zero, Round up, Round down, Round Nearest to Infinity and Round Ties to Even.
- Supports the exceptions: Div-by-zero, Infinity, Inexact, overflow and underflow.
- Supported operations are:
  - Half, Single and double precision addition/subtraction.
  - Half, Single and double precision multiplication.
  - Half, Single and double precision multiply-accumulate. Half, Single and double precision division and square-root.
  - Half, Single and double precision Posit comparator.
  - Half precision Posit to signed or unsigned integer conversion.
  - Single precision Posit to signed or unsigned integer conversion.
  - Double precision Posit to signed or unsigned integer conversion.
  - Unsigned Integer (32/64-bit) to half precision Posit conversion.
  - Unsigned Integer (32/64-bit) to single precision Posit conversion.
  - Unsigned Integer (32/64-bit) to double precision Posit conversion.
  - Signed Integer (32/64-bit) to half precision Posit conversion.
  - Signed Integer (32/64-bit) to single precision Posit conversion.
  - Signed Integer (32/64-bit) to double precision Posit conversion.
  - Posit movement operations.
  - Half precision Posit sign injection operations.
  - Single precision Posit sign injection operations.
  - Double precision Posit sign injection operations.
  - Posit to Posit Conversion operations.
- Verification Strategies adopted:
  - Using Random vectors.
  - IBM FPGen floating point test-suite converted to Posit.
  - Berkley Test float test cases converted to Posit.
  - Coverage model based PositGen vectors.
- Synthesized and tested targeting Virtex UltraScale VCU 118 FPGA development board.

4. Application Areas + Benefits of the product

The RISC-V Instruction Set Architecture Enabled Posit Arithmetic Unit IP Core may be used in the following application scenarios:

- Alternate for IEEE 754 based FPU in RISC-V based Microprocessor.
- Posit Arithmetic Unit for RISC-V based embedded class processor.
- As FPGA based Posit computation accelerators for embedded class applications.
- Processing Element for AI/ML accelerator.
- General purpose audio and video processing applications.
- Processing Elements for Financial Transactions based applications.

Since the IP core will be provided in source-code (Verilog) form, it'll enable the end-user to modify / enhance / customize Posit RTL IP core for future needs based on the application scenarios.

5. Technology Transfer

The technology will be transferred as non-exclusive basis. The technology fee will be finalized at a later stage. The ToT package contains the following:

1. User-reference guide for individual Posit floating point operation with block-level explanation of IP core, and interfacing details.
2. High Level and Low Level Design Documents.
3. RTL source-code – Verilog source code.
4. Test benches, Test Results, Test Bench Design Documents and Test Reports
5. Scripts for synthesis.
6. Scripts for simulation.
7. Handholding support for a period of 6 months.

6. General terms and conditions

i. An expert committee will scrutinize the applications for follow-up action.
ii. The applicants may be called for a presentation regarding their strengths and business proposals.
iii. All incidental expenditure incurred in preparation/ submission or presentation of the EoI shall be borne by the participating agency.
iv. Participation in this EoI does not guarantee any association with C-DAC unless notified by C-DAC in writing.
v. The design of the IP, shared by C-DAC to the establishment receiving the ToT, will be final. No further changes / revisions / enhancements by C-DAC will be considered.
vi. C-DAC reserves the right of rejecting any offer without assigning reasons.
vii. Last date for submission of EoI is 45 days from issue of the first advertisement. Any offer received after due date and time will not be accepted.
viii. There is neither a business guarantee nor any commitment for funding support from C-DAC to the appointed/ empanelled agencies.
ix. A Committee of experts constituted by C-DAC will assess capabilities and strengths of the industry before finalizing the technology partners.
x. The industry willing to take technology for commercial exploitation will be required to enter into a ToT agreement with C-DAC as per the terms and conditions approved by the competent authority in C-DAC / in the MeitY in the prescribed format.

7. Who can apply?

- Establishments offering FPGA based design solutions, arithmetic unit hardware IP cores for embedded class processors, FP computations as functional units for an existing embedded class processor, establishments designing RISC-V ISA based processors, etc.
- Establishments with interest in Electronics or Information and Communications Technology (ICT).

- Establishments willing to take up the adoption, production and proliferation of RISC-V ISA enabled Posit Arithmetic Unit IP core as per the ToT guideline agreement of C-DAC.

Establishments having years of industry expertise in areas related to: hardware IP cores, arithmetic core modelling and design, Floating Point computational Units, processor / co-processors for arithmetic computations, softcore processor based design, FPGA based high performance computing accelerators, etc. having good experience in design and development of complex FPGA based digital design can apply. Expected capabilities are detailed in table below:

Expected Capabilities	**Expected & related Skillsets/ Technologies**
Expertise on HDL languages EDA Tools	Verilog, VHDL, Xilinx XST Design/ Implementation Flow.
Domain Knowledge	Arithmetic unit - modelling and design, Floating Point Unit, Co-processor design, ASIC / FPGA.
Programmable Device	FPGA device internals and development on FPGAs.

8. How to apply?

Interested establishments may send expression of interest with their details by filling the questionnaire as per Annexure–I (Part A and Part B) along with supporting documents to:

The Executive Director
Centre for Development of Advanced Computing
C-DAC Knowledge Park,
Opp. HAL Aeroengine Division, No.1 Old Madras Road
Byappanahalli, Bengaluru - 560 038. Karnataka (India)
Phones: +91-80-25093400
Fax: +91-80-2524-7724

9. Expression of Interest

a) C-DAC invites “Expression of Interest” in the format given in Annexure-I (Part A & Part B). The industries will be shortlisted based on the information furnished in Annexure–I and assessment by the ToT committee.

b) The submission of the EOI shall include all such documents that are specified herein to prove the authenticity of their offer and any claim made therein. The burden of proving such claims shall lie with the bidder.

c) All cost and expenses associated with submission of EOI shall be borne by the bidder while submitting the EOI and C-DAC shall have no liability, in any manner in this regard, or if it decides to terminate the process of short listing for any reason whatsoever.

Annexure-I (Part A)

The following details should be submitted along with the EOI by the bidder

A	**Company Profile**
1.	Name of the Organization: Website:
2.	Details of the Contact Person: Name: Address: Telephone: Fax: E-Mail:
3.	Year of Incorporation:
4.	Type of Organization: a) Public Sector/ Limited/Private Limited/ Partnership/ Proprietary/ Society/Any other b) Whether 'Foreign Equity Participation (Please give name of foreign equity participant and percentage thereof) c) Names of Directors of the Board/ Proprietors d) Name and address of NRI(s), if any
5.	Category of the firm: Large/Medium/Small scale unit
6.	Address of the Registered Office:
7.	Number of Offices with addresses (Excluding Registered Office): India:_____ Abroad:_____
8.	Certificate of registration as: (Please specify one of the following, as applicable) a) A Manufacturing Unit b) Hardware / System Design Services Unit c) R&D Establishment / Organization d) Hardware / System Design Company / Organization e) Any Others (bidder to mention)
9.	Permanent Account Number:
10.	Sales Tax Number/ VAT:
11.	Status of ISO9001/ISO13485 (or equivalent) Certification:

Annexure-I (Part B)

B	Essential Requirement
1.	The organization must be a reputed firm/company/SME/startup/R&D company incorporated in India with standing of at least 2 years.
2.	The turnover is to be a supported by financial statements of accounts/Annual reports duly certified by a Chartered accountant/Balance sheets of last 2 years/Income tax returns for the last 2 years period.
3.	Company profile, giving details of current activities and management/personnel structure including evidence of incorporation. The company should be registered and preferably ISO 9001or equivalent certified.
4.	Details of absorption of technology for a product/knowhow that has been taken up on production scale in the past may also be given.
5.	The manpower strength (Technical: Mechanical, Electrical, Electronics, Software & Non-Technical etc.) at various levels to be furnished. Technical: a. B.E./B. TECH/MTech/MS/MSc/PhD/any other b. DIPLOMA/PG Diploma c. SKILLED TECHNICIANS d. UNSKILLED/SEMI SKILLED
6.	The list of equipments / software / hardware / facilities available related with work to be furnished.
7.	The in-house technological expertise available to be furnished.
8.	The list of equipments / hardware systems / tools available for design and development / testing / verification / validation / inspection and quality control of systems / hardware / firmware etc. to be furnished.
9.	The industry should have adequate space for undertaking this work. Available office space-Covered & Open to be furnished.
10.	List of products/technologies worked with as regular activity in last two years. Give the list of products/technologies with general specifications and the customers.
11.	List of PSUs/Govt. Customers, if any – with contact details (Address, Telephone no., Contact Person).
12.	The details of design and development, design services, product design, sales / business development, marketing and maintenance / Customer support network to be furnished.
13.	The list of technical collaborations for various ongoing products may be furnished, if any.
C.	**Expression of Interest: Spell out the extent of interest**

I hereby declare that the above information is true to the best of my knowledge.

Signature with Name & Seal:

Place:
Date:

Note: Expression of interest should be stamped and signed by authorized signatory with a formal declaration note.