CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING

Knowledge Park, Bangalore

Date: May 06, 2022

Minutes of Pre-bid meeting (Online) held on 06.05.2022 through https://sangoshthee.cdac.in/BDGBangalore

Ref: Notice Inviting Expression of Interest - EOI No. C-DAC (KP)/TOT/2021-2022 dated 14.04.2022 from competent companies for Commercialization of RISC-V ISA compliant Floating-Point Unit (High Performance) IP Core, RISC-V ISA compliant Floating-Point Unit (Lite) IP core and RISC-V ISA compliant POSTIT Arithmetic IP core.

1. Queries raised by the prospective bidders and the clarifications are as follows:

Sr.No	Non-Technical Queries	Clarification
1.	Is there any kind of Non-Disclosure agreement to be signed with CDAC?	NDA explicitly need not be signed. TOT agreement that will be signed with the selected bidders includes NDA as one of the clauses.
2.	In the financial bids, since it is not on exclusive basis, there will be business risks involved. As there can be multiple bidders with similar pricing, how are the bidders selected?	The TOT policy is on a non-exclusive basis, enabling multiple bidders to be selected and get the transfer of technology. Bidder with the highest bid will be selected and other interested bidders will be asked to match the highest bid price.
3.	Is there any minimum price expected?	Currently this is an expression of interest, where the bidders are asked to submit EOIs. Once the EOI's are screened, the shortlisted bidders will be informed of the minimum price and asked to submit the bids. Bidders with the highest bid will be selected for TOT.
4.	How many bidders will be selected, or is that one with the highest bid will be selected and others will be asked to match the highest bid??	The TOT policy is on a non-exclusive basis, enabling multiple bidders to be selected and get the transfer of technology. Bidder with the highest bid will be selected and other interested bidders will be asked to match the highest bid price.

5.	We are a start-up company. Is the ISO Certificate mandatory.	The EOI asks for the status of ISO Certifications. EOI from bidders without ISO certification also will be considered.
6	Is the bidding to be completed today or is there any time period?	Currently this is an expression of interest, where the bidders are asked to submit EOIs. Once the EOIs are screened, the shortlisted bidders will be informed of the minimum price and asked to submit the bids. The last date for submission of EOI is 30th May 2022.

Sr.No	Technical Queries	Clarification
1	Is design targeted for any specific technology node?	Presently, the design is not targeted for any specified technology node. Since the design is in RTL, it can be taken further in ASIC flow targeting any technology node.
2.	Is the design taken through Physical Design flow?	No. The designs have been currently validated on UltraSclace+ VCU 118 using Xilinx Vivado Synthesis and Implementation FPGA flow.
3.	Is the design targeted for automotive applications? During design phase any consideration was given to the IP core to target it for automotive applications?	The IP cores have not been developed based on any specific design constraints related to automotive applications.
4.	The current code is tested for the core functionality on FPGA, so along with code what are the other peripherals tested with IP core?	The Posit/FPU IP cores have been integrated as functional units with the RISC-V Processor core developed in System Verilog. The Core is integrated in a SoC framework consisting of Level-1 Instruction & Data Caches, AXI interconnect, UART, CLINT and Block RAM based Main Memory.
5.	Is the RISC-V processor core used for integration and testing of Posit/FPU based on open-source?	No, the 6-stage pipelined RV64IMAFD RISC-V

		Processor Core has been developed in System Verilog. The Posit/FPU IP cores have been integrated and tested as functional units in the processor core.
6.	Any benchmarking is performed with Posit IP core?	We have not yet done any application benchmarking for Posit IP core. Area and frequency analysis on FPGA were done for the Posit IP core.
7.	What will be the procedure for Demo in lab? Will the demo be done in a weeks' time?	Yes. Demo can be arranged based on request via e-mail.
8.	Does the Posit IP core have a high performance variant?	No, currently only IEEE-754 FPU has a high-performance variant – FPU (high-performance).
9.	Will C-DAC deliver compiler modifications also as part of ToT package?	The ToT package includes the modified RISC-V software toolchain for enabling POSIT data representation instead of IEEE -754.
10.	How much is the complexity for migrating IP cores to silicon?	Since, IP cores are available in RTL, it can be taken further in ASIC flow targeting any specific technology node. Currently, the developed IP cores have been validated on UltraSclae+ VCU 118 FPGA using Xilinx Vivado Synthesis and Implementation flow.
11.	Does C-DAC have any indicating performance numbers for FPU lite, FPU High Performance and Posit IP core?	Yes, area (LUT and Register) utilization and frequency figures for FPGA devices are available. The information can be shared based on request via email.
12.	What are the assumptions chosen for clock cycles for critical path?	For each submodule of FPU & Posit, the clock cycles are decided based on its complexity of operation and balancing of the combinational path across pipeline stages.

13.	Is the design FPGA specific?	No, the designs do not use FPGA specific primitives. The developed IP cores are RTL codes developed using Bluespec System Verilog (BSV) (FPU High-Performance and Lite variants) and Verilog (Posit).

Sd/-
Committee Members